

Evaluation of a Low Frequency Clock Oscillation Circuit

SSP-T7-F 7.0pF with uPD78F0588GA-48P [LQFP(7x7) 0.5mm pitch]

Measurement conditions : 3.0V

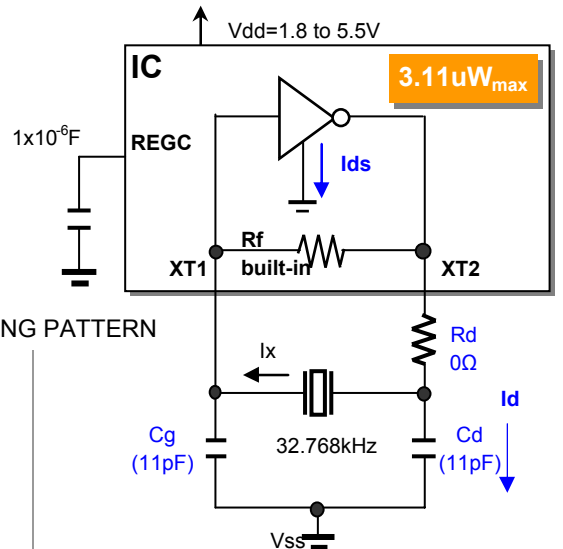
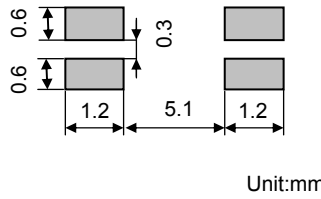


Model : SSP-T7-F
 Frequency : Fo=32.768kHz
 Frequency tolerance : dF/Fo= +/-20x10⁻⁶
 Load capacitance : CL=7.0pF
 Equivalent series resistance : R1=65kohm max
 Max. drive level : DL=1 μW max
 Level of drive : DL=0.1μW typ

FEATURES

- 1.Ultra thin type with 1.4mm Max.
- 2.SMD type suitable for automatic & high density surface mounting.
- 3.Plastic mold package containing highly reliable tubular type quartz crystal.
- 4.Excellent shock and heat resistance.
- 5.Cellular phones,PDA, Radio communication equipment, Portable applications etc.

RECOMMENDED SOLDERING PATTERN



Remark) I_x : current through crystal
 I_{sub}=I_{ds}+I_d : current consumption

	REGVDD	Oscillation mode
Mode 1	2.4V	Normal (*1)
Mode 2	2.0V	

Normal power consumption 78K0/KC2-L and SSP-T7-F 7.0pF

Normal current consumption of the XT1 oscillation circuit is I_{sub} (=1.597μA typ).

***1 ; Normal current consumption mode**

MODEL:SSP-T7-F 7.0pF with uPD78F0588GA at 25°C

Key specifications	Mode 2	Mode 1	Remarks
Current control resistance : Rd (kΩ)	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	11	11	Optimal capacitance in response to CL
Capacitance at drain : Cd (pF)	11	11	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Mode 2	Mode 1	Remarks
Matching Accuracy : df / f (x10 ⁻⁶)	-1.8	-1.7	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V (x10 ⁻⁶)	0.0	0.0	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL (nW)	21.3	21.3	DL=Ix ² Re < 1x10 ⁻⁶ W, Re=R1(1 + Co / CL) ²
Negative resistance : - RL (kΩ)	608	608	5 times larger than R _{1MAX}
Oscillation allowance : M (times)	9	9	Judgmental standard of oscillation stability
Normal current consumption : I _{sub} (μA)	1.462	1.457	I _{sub} = Id + I _{ds} = ωCd*Vd + 1/2* gm(Vg-V _{TH})
Cd charge current : Id (μA)	0.398	0.398	Cd charge current, Id = ωCd*Vd
Voltage of oscillation start : Vstrat (V)	1.57	1.57	
Oscillation start up time : Ts (sec)	0.83	0.83	Time to reach 90% of output level, Ts< 1.5sec

Temperature characteristics of circuit		Mode 2	Mode 1	Remarks
at -40°C	Variation : df / T (x10 ⁻⁶)	-141	-141	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)
at +85°C	Variation : df / T (x10 ⁻⁶)	-128	-128	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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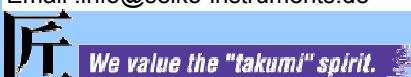
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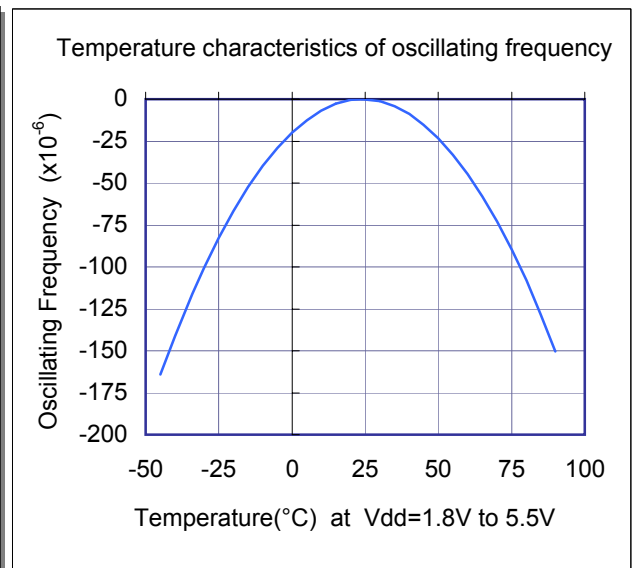
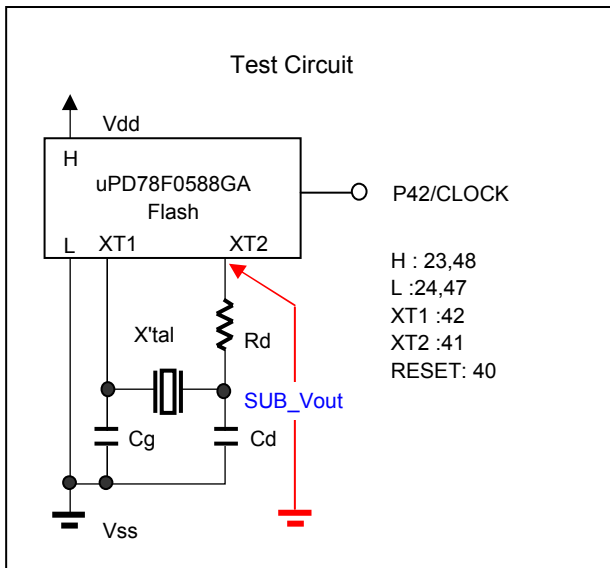
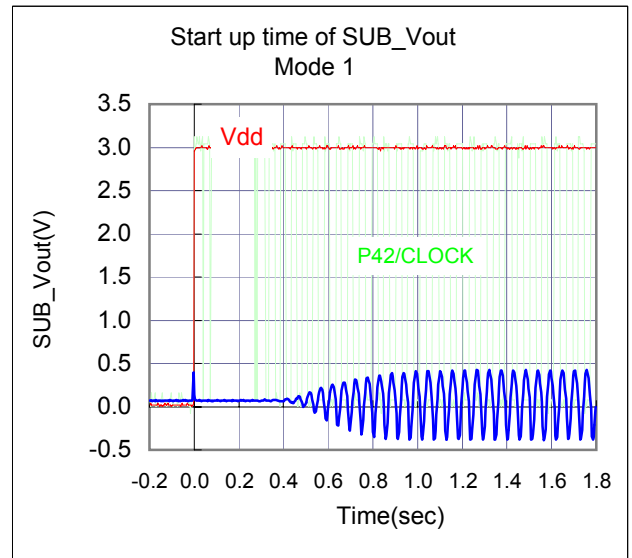
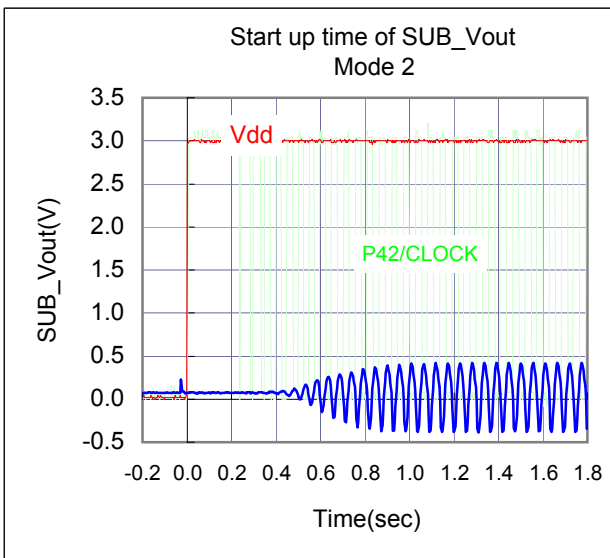
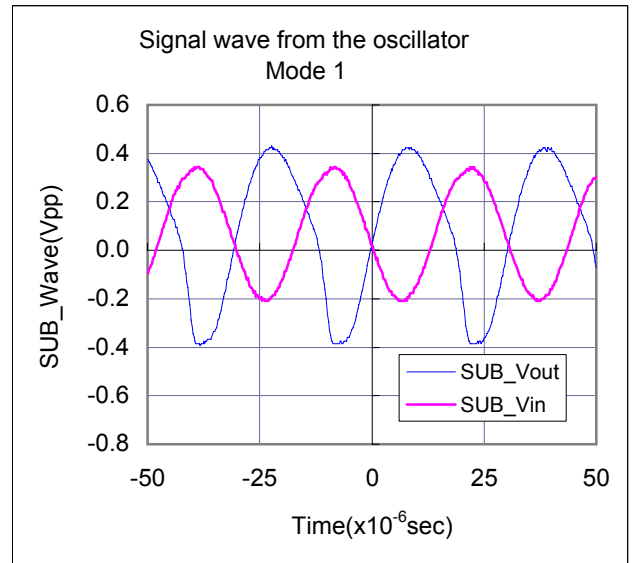
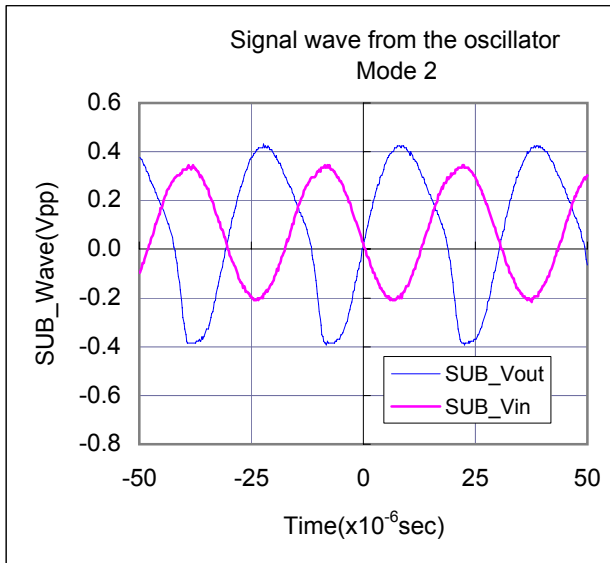
SSP-T7-F 7.0pF with uPD78F0588GA-48P [LQFP(7x7) 0.5mm pitch]

Measurement conditions : 3.0V



Normal current consumption mode

Test Data at 25°C



Evaluation of a Low Frequency Clock Oscillation Circuit

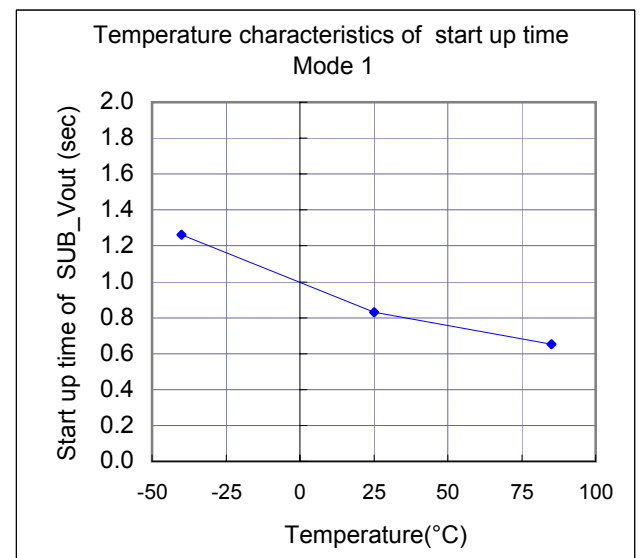
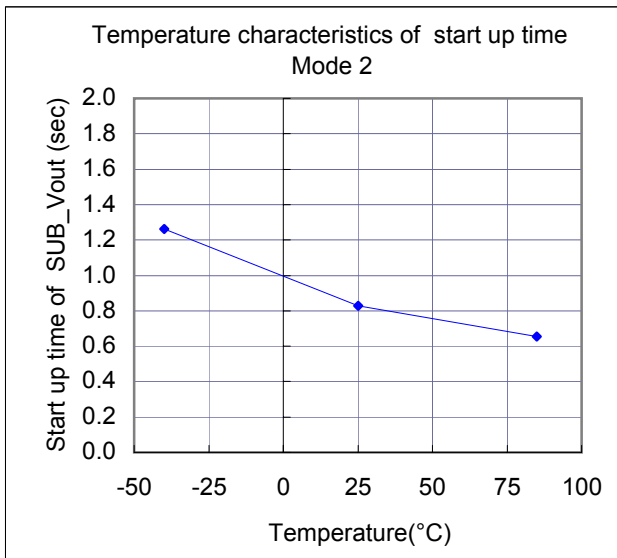
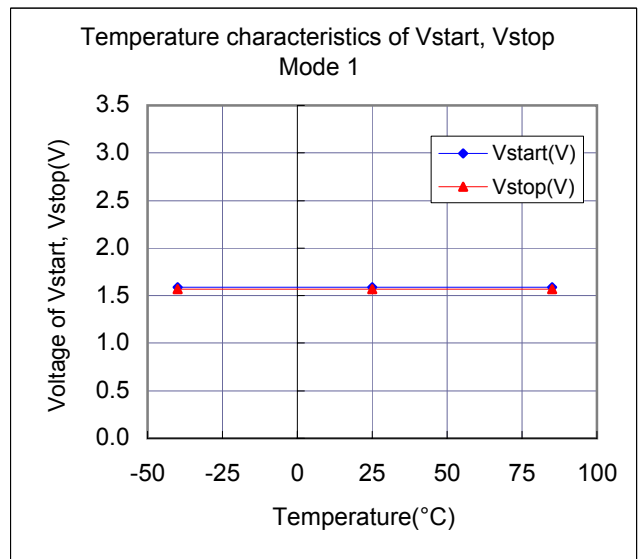
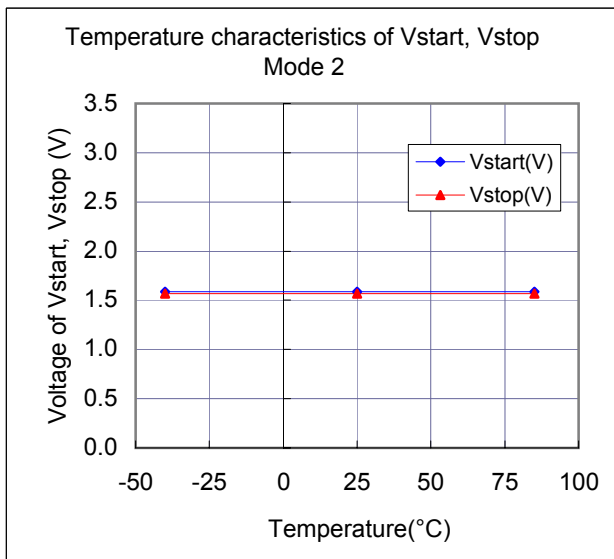
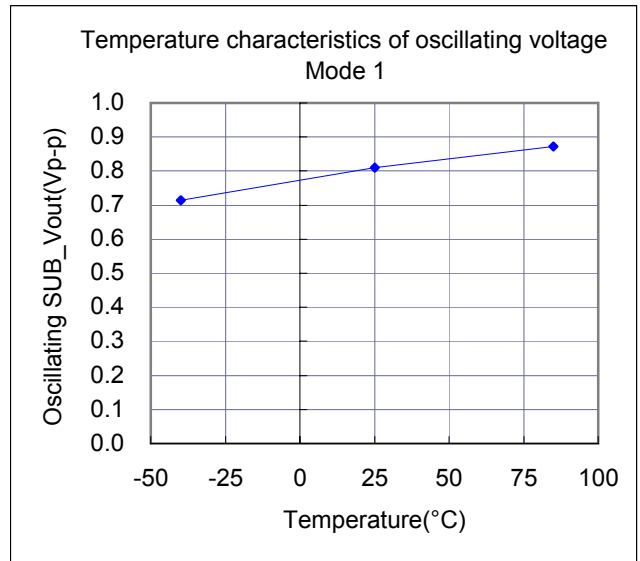
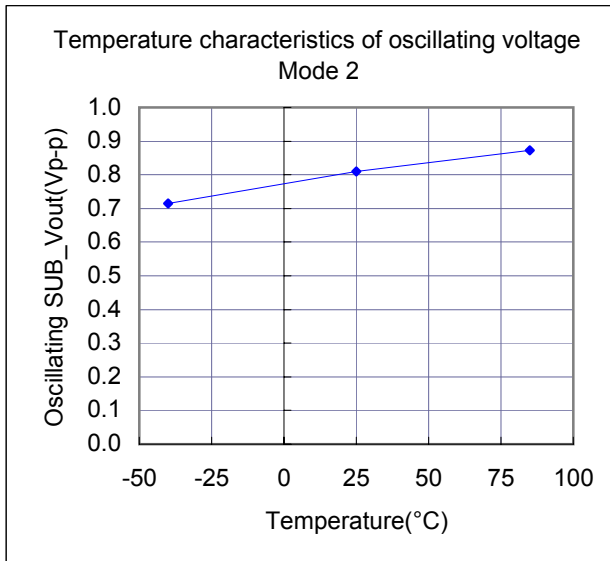
SSP-T7-F 7.0pF with uPD78F0588GA-48P [LQFP(7x7) 0.5mm pitch]

Measurement conditions : 3.0V



Normal current consumption mode

Test Data : Temperature characteristics



Evaluation of a Low Frequency Clock Oscillation Circuit

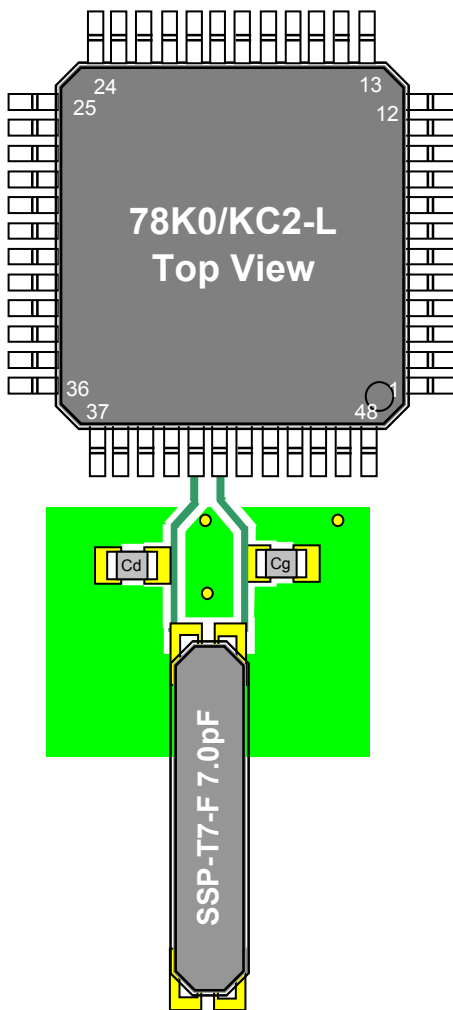
SSP-T7-F 7.0pF with uPD78F0588GA-48P [LQFP(7x7) 0.5mm pitch]

Measurement conditions : 3.0V



Normal current consumption mode

Referential components layout(see Figure 1)



78K0/Kx2-L series

78K0/KC2-L

- uPD78F0581GA (48pin)
- uPD78F0582GA (48pin)
- uPD78F0583GA (48pin)
- uPD78F0586GA (48pin)
- uPD78F0587GA (48pin)
- uPD78F0588GA (48pin)
- uPD78F0581GB (44pin)
- uPD78F0582GB (44pin)
- uPD78F0583GB (44pin)
- uPD78F0586GB (44pin)
- uPD78F0587GB (44pin)
- uPD78F0588GB (44pin)

MODEL: SSP-T7-F 7.0pF with uPD78F0588GA at 25°C

AMPHS1	AMPHS0	on mode selection
0	0	Low consumption oscillation mode. (default); Isub=0.698μA typ.
0	1	Normal consumption oscillation mode. Isub=1.597μA typ.
1	0	Extremely low consumption oscillation mode. *N/R
1	1	Extremely low consumption oscillation mode. *N/R

Current consumption of the XT1 oscillation circuit is equal to Isub.

*N/R: Not recommended.(underestimated gain at 7.0pF)

Figure 1 Referential components layout

Notes for Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

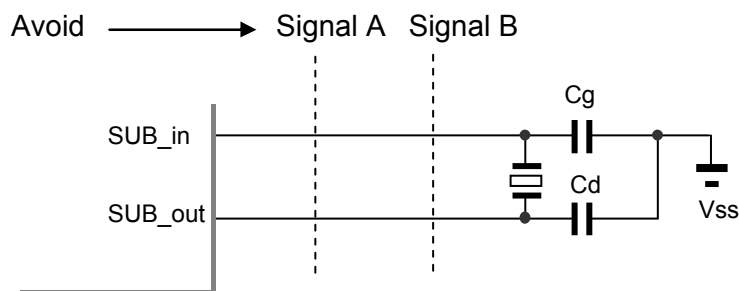


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert a resistor, Rd, in series on the SUB_out side.

Evaluation of a Low Frequency Clock Oscillation Circuit

SSP-T7-F 7.0pF with uPD78F0588GA-48P [LQFP(7x7) 0.5mm pitch]

Measurement conditions : 3.0V



Normal current consumption mode

[Evaluation Sample at 25°C]

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
SSP-T7-F	1	7.0	32767.91	32763.64	41.0	0.89	2.058	57.6
	2	7.0	32768.10	32763.71	37.5	0.90	2.117	61.2
	3	7.0	32768.33	32763.94	35.9	0.90	2.117	63.9

[IC Test Data : IC sample Rd=0Ω,Cg=11pF,Cd=11pF at 25°C]

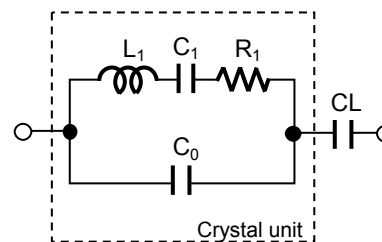
MODE	IC sample	df / f(x10 ⁻⁶)	DL(nW)	RL(kΩ)	M(times)	XT2(Vpp)	Id(μA)	Vstart(V)	Ts(sec)
Mode 1 (2.4V)	Sample 1	-1.7	32.0	-668	10	0.88	0.43	1.58	0.99
	Sample 2	-1.6	32.3	-668	10	0.92	0.45	1.59	0.97
	Sample 3	-2.1	20.5	-608	9	0.81	0.40	1.58	0.89
	Sample 4	-1.7	21.3	-608	9	0.81	0.40	1.59	0.83
AVG.		-1.79	26.5	-638	9.8	0.86	0.421	1.59	0.92

[IC Test Data : IC sample Rd=0Ω,Cg=11pF,Cd=11pF at 25°C]

MODE	IC sample	df / f(x10 ⁻⁶)	DL(nW)	RL(kΩ)	M(times)	XT2(Vpp)	Id(μA)	Vstart(V)	Ts(sec)
Mode 2 (2.0V)	Sample 1	-1.9	32.0	-668	10	0.88	0.43	1.58	0.99
	Sample 2	-1.7	32.4	-668	10	0.92	0.45	1.59	0.97
	Sample 3	-2.2	20.5	-608	9	0.81	0.40	1.58	0.89
	Sample 4	-1.8	21.3	-608	9	0.81	0.40	1.59	0.83
AVG.		-1.90	26.6	-638	9.8	0.86	0.421	1.59	0.92

Remark (see figure 3)

$$F_o = f_r \times \left\{ \frac{C_1}{2 \times (C_o + C_L)} + 1 \right\} \text{ (Hz)}$$



Fo : Load resonance frequency
fr : Resonance frequency
R1 : Motional resistance
C1 : Motional capacitance
Co : Shunt capacitance
CL : Load Capacitance

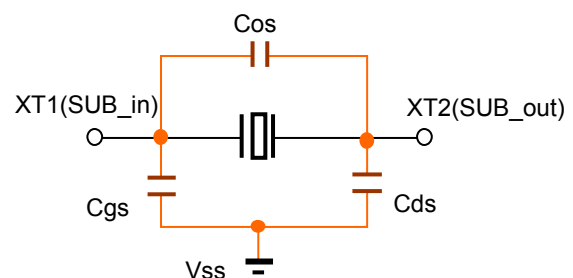
Figure 3 Equivalent circuit of crystal unit, and CL**Remark (see figure 4)**

Approximate formula of the load capacitance of the circuit CL,

$$C_L = C_g \times C_d / (C_g + C_d) + C_s \text{ (pF)}$$

$$C_s = C_{gs} \times C_{ds} / (C_{gs} + C_{ds}) + C_{os} \text{ (pF)}$$

where Cs(1.5 to 2.5pF) stands for stray capacitance of the circuit.



Cos : X1_X2 Stray capacitance
Cgs : X1_Vss Stray capacitance
Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

Evaluation of a Low Frequency Clock Oscillation Circuit

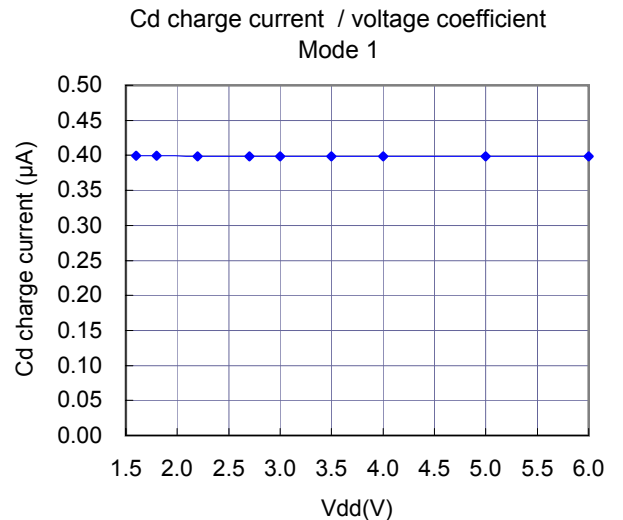
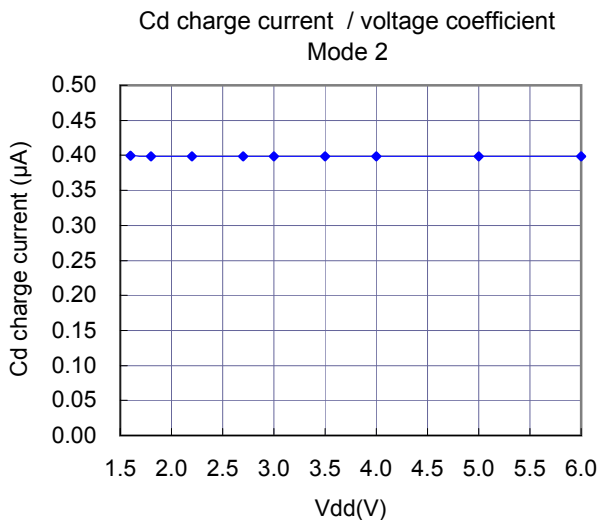
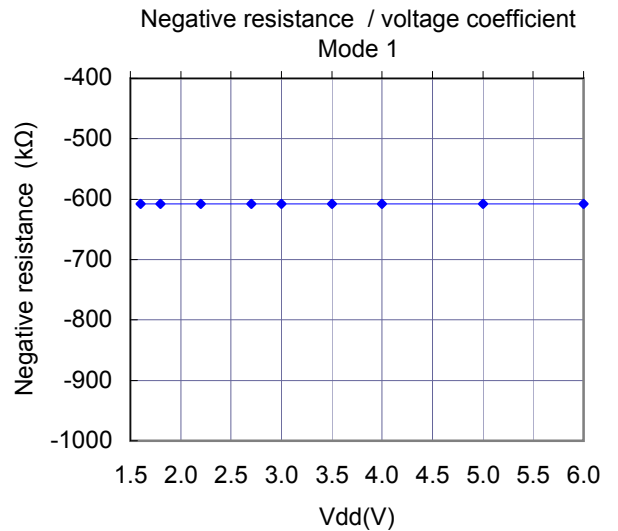
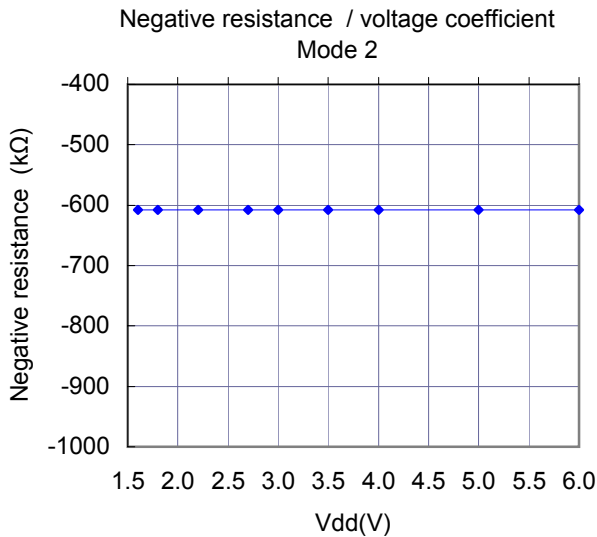
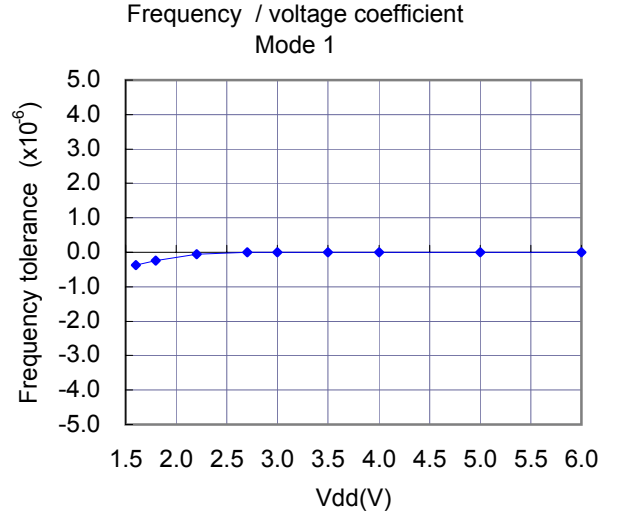
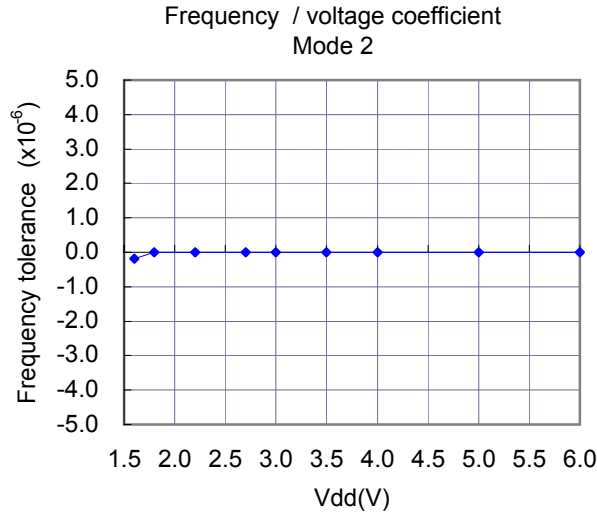
SSP-T7-F 7.0pF with uPD78F0588GA-48P [LQFP(7x7) 0.5mm pitch]

Measurement conditions : Vcc=(1.6V) to (6.0V) at 25°C



Normal current consumption mode

Referential Data(1) : Voltage characteristics



Evaluation of a Low Frequency Clock Oscillation Circuit

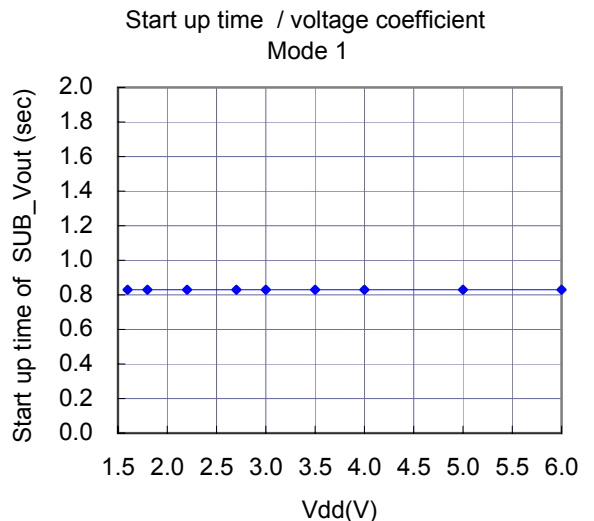
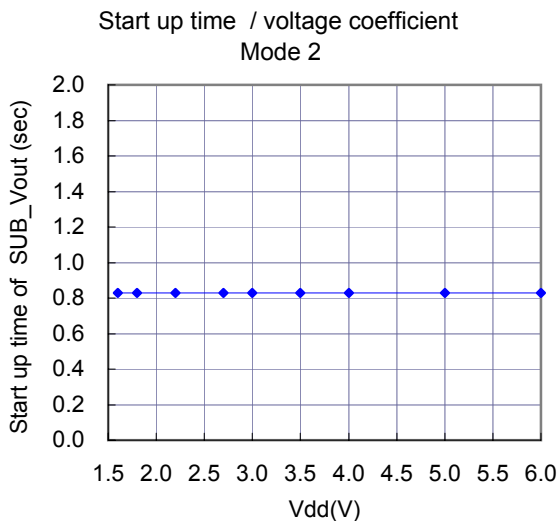
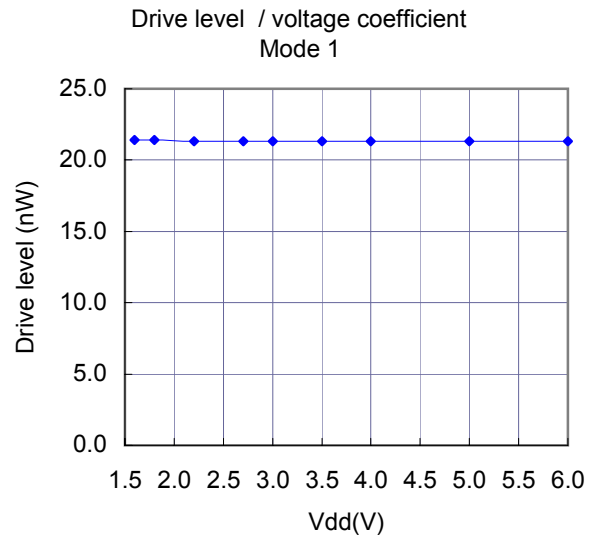
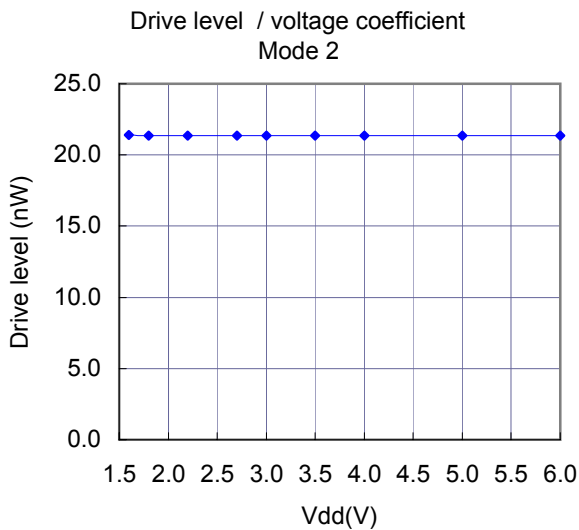
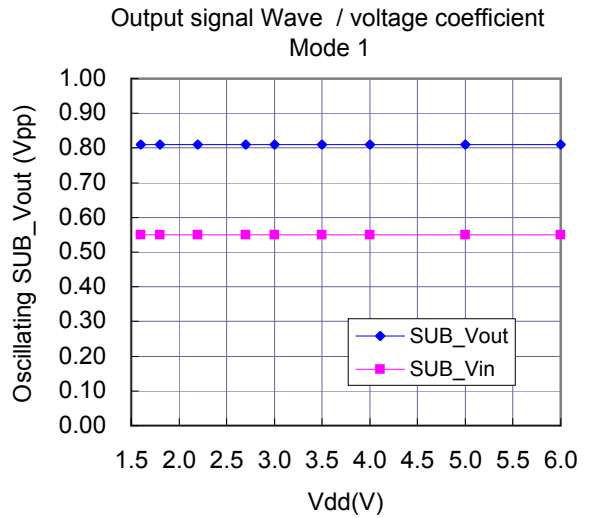
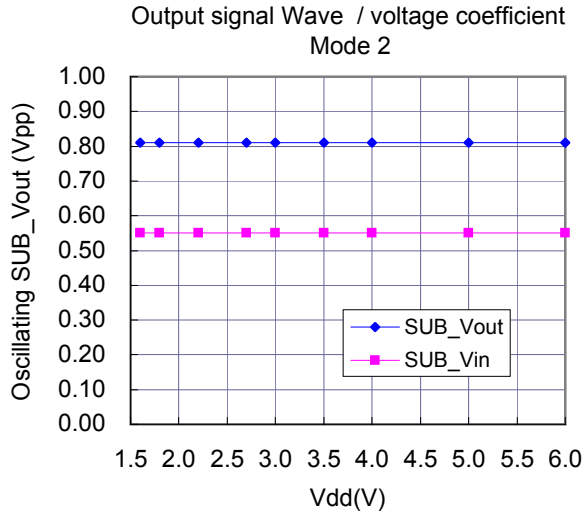
SSP-T7-F 7.0pF with uPD78F0588GA-48P [LQFP(7x7) 0.5mm pitch]

Measurement conditions : Vcc=(1.6V) to (6.0V) at 25°C



Normal current consumption mode

Referential Data(2) : Voltage characteristics



Evaluation of a Low Frequency Clock Oscillation Circuit

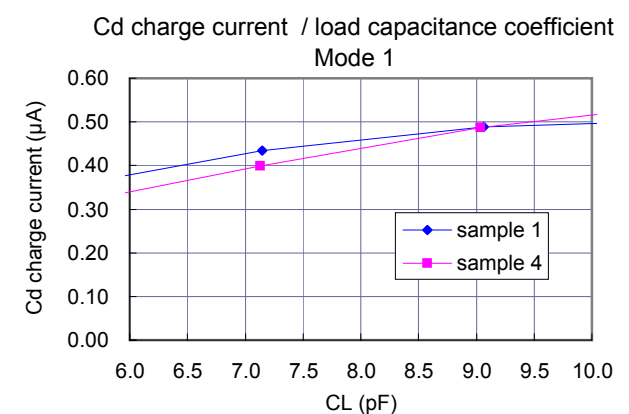
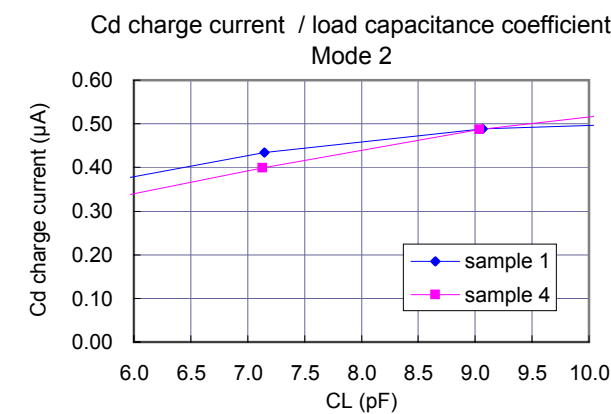
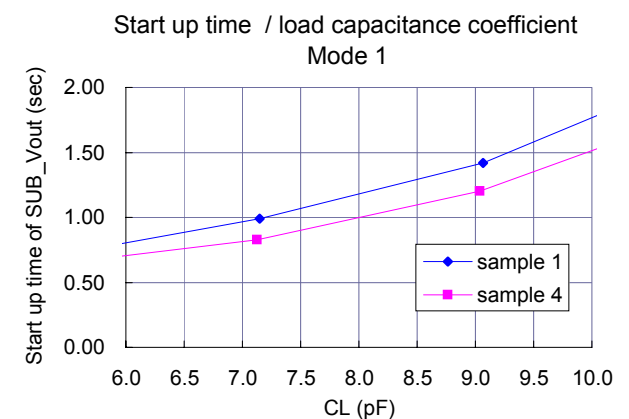
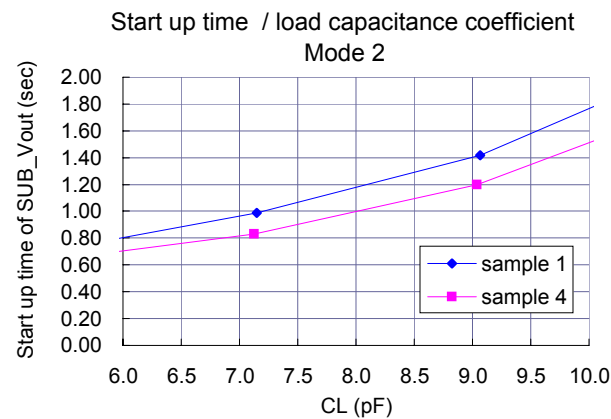
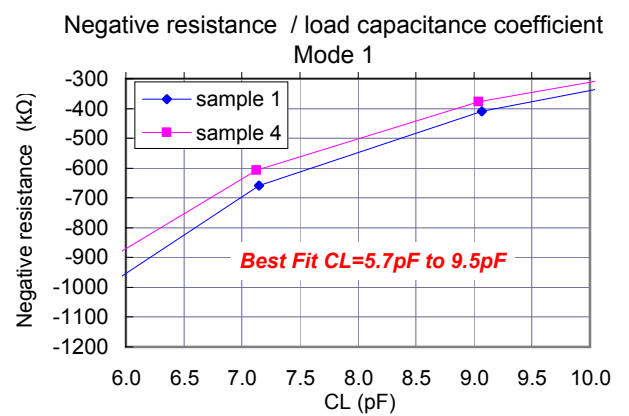
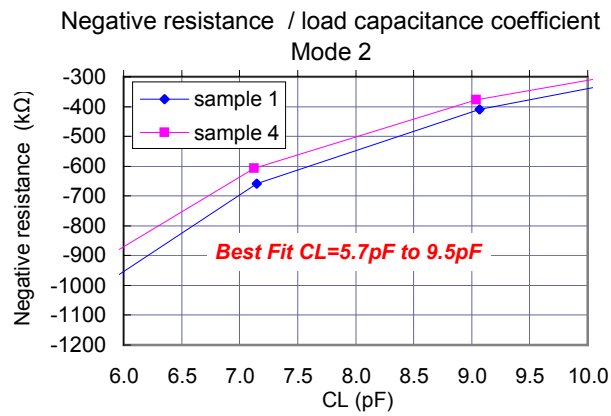
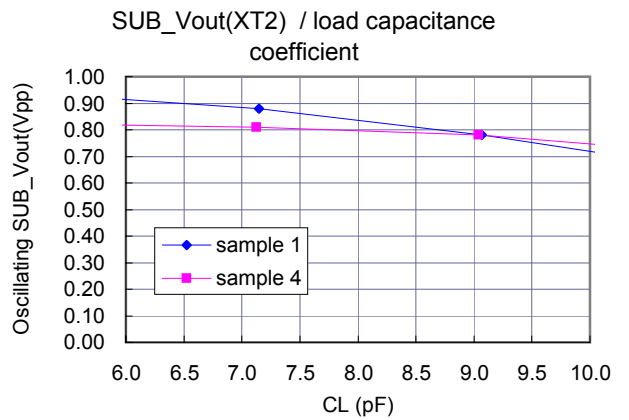
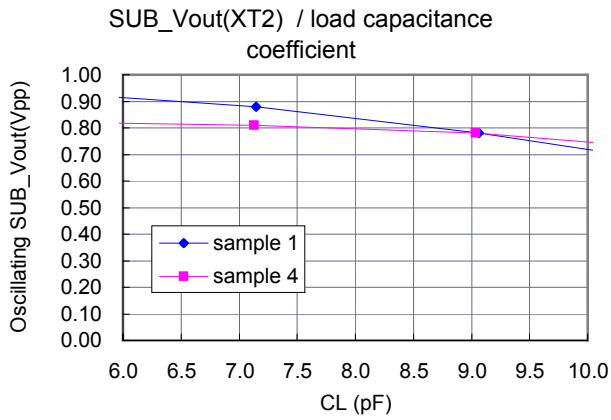
SSP-T7-F 7.0pF with uPD78F0588GA-48P [LQFP(7x7) 0.5mm pitch]

Measurement conditions : Vdd=3.0V at 25°C



Normal current consumption mode

Referential Data(3) : Load capacitance characteristics



Evaluation of a Low Frequency Clock Oscillation Circuit

SSP-T7-F 7.0pF with uPD78F0588GA-48P [LQFP(7x7) 0.5mm pitch]

Measurement conditions : V_{dd}=3.0V at 25°C

Normal current consumption mode

Referential Data(4) : IC sample characteristics(Normal mode)



Table 1 Oscillation mode selection of XT1 oscillation circuit and load capacitance for a resonator

AMPHS1	AMPHS0	Oscillation mode selection ^{*2}	Recommended CL (Current consumption; I _{sub} ^{*3})
0	0	Low consumption oscillation mode.(default)	4.4pF (0.634μA),6.0pF (0.675μA typ)
0	1	Normal consumption oscillation mode.	7.0pF (1.597μA typ),9.0pF (1.677μA typ)
1	0	Extremely low consumption oscillation mode.	3.7pF(0.262μA typ),4.4pF (0.279μA typ)
1	1	(DC bias current; 200nA max. at 25°C)	

*2)78K0/KC2-L ; μPD78F0581 to μPD78F0588 & SSP-T7 series.

*3)Current consumption of the XT1 oscillation circuit is equal to I_{sub}.**Normal current consumption mode; IC sample Rd=0Ω,Cg=11pF,Cd=11pF,CL=7.0pF**

MODE	IC sample	df / f(x10 ⁻⁶)	CL(pF)	Cs(pF)	M(times) ^{*4}	I _{sub} (μA)	I _{ds} (μA)	I _d (μA)	T _s (sec)
Mode 1 (2.4V)	Sample 1	-1.7	7.1	1.6	10	1.72	1.28	0.43	0.99
	Sample 2	-1.6	7.1	1.6	10	1.73	1.28	0.45	0.97
	Sample 3	-2.1	7.1	1.6	9	1.48	1.07	0.40	0.89
	Sample 4	-1.7	7.1	1.6	9	1.46	1.06	0.40	0.83
Mode 2 (2.0V)	Sample 1	-1.9	7.1	1.6	10	1.72	1.29	0.43	0.99
	Sample 2	-1.7	7.1	1.6	10	1.73	1.28	0.45	0.97
	Sample 3	-2.2	7.1	1.6	9	1.48	1.08	0.40	0.89
	Sample 4	-1.8	7.1	1.6	9	1.46	1.06	0.40	0.83
AVG.		-1.84	7.11	1.61	9.8	1.597	1.176	0.421	0.92

*4)R1max=65kΩ

Normal current consumption mode; IC sample Rd=0Ω,Cg=9pF,Cd=8pF,CL=6.0pF

MODE	IC sample	df / f(x10 ⁻⁶)	CL(pF)	Cs(pF)	M(times) ^{*4}	I _{sub} (μA)	I _{ds} (μA)	I _d (μA)	T _s (sec)
Mode 1 (2.4V)	Sample 1	2.0	5.9	1.6	15	1.67	1.29	0.39	0.87
	Sample 2	2.1	5.9	1.6	15	1.68	1.28	0.40	0.86
	Sample 3	1.8	5.9	1.6	13	1.41	1.06	0.34	0.76
	Sample 4	2.4	5.9	1.6	14	1.41	1.07	0.35	0.72
Mode 2 (2.0V)	Sample 1	1.9	5.9	1.6	15	1.68	1.29	0.39	0.87
	Sample 2	2.0	5.9	1.6	15	1.69	1.28	0.40	0.86
	Sample 3	1.6	5.9	1.6	13	1.41	1.07	0.34	0.76
	Sample 4	2.3	5.9	1.6	14	1.42	1.07	0.35	0.72
AVG.		2.03	5.91	1.62	14.2	1.547	1.176	0.370	0.80

*4)R1max=65kΩ

Normal current consumption mode; IC sample Rd=0Ω,Cg=15pF,Cd=15pF,CL=9.0pF

MODE	IC sample	df / f(x10 ⁻⁶)	CL(pF)	Cs(pF)	M(times) ^{*4}	I _{sub} (μA)	I _{ds} (μA)	I _d (μA)	T _s (sec)
Mode 1 (2.4V)	Sample 1	-1.3	9.1	1.6	6	1.78	1.29	0.49	1.41
	Sample 2	-1.1	9.1	1.6	6	1.80	1.28	0.52	1.40
	Sample 3	-1.3	9.1	1.6	6	1.54	1.04	0.49	1.33
	Sample 4	-1.0	9.1	1.6	6	1.58	1.09	0.49	1.21
Mode 2 (2.0V)	Sample 1	-1.4	9.1	1.6	6	1.78	1.29	0.49	1.41
	Sample 2	-1.2	9.1	1.6	6	1.81	1.29	0.52	1.40
	Sample 3	-1.4	9.1	1.6	6	1.54	1.05	0.50	1.33
	Sample 4	-1.1	9.1	1.6	6	1.59	1.09	0.49	1.21
AVG.		-1.24	9.11	1.61	6.0	1.677	1.177	0.500	1.34

*4)R1max=65kΩ

Evaluation of a Low Frequency Clock Oscillation Circuit

SSP-T7-F 7.0pF with uPD78F0588GA-48P [LQFP(7x7) 0.5mm pitch]

Measurement conditions : Vdd=3.0V at 25°C



Normal current consumption mode

Referential Data(5) : Selection of XT1 oscillation mode and recommended load capacitance

For 78K0/KC2-L

XT1 oscillation circuit has the function (via software) to select the XT1 oscillation mode.

The XT1 oscillation mode can be switched over just one time among normal oscillation (**Normal**), low consumption oscillation (Low), and "extremely low consumption oscillation" mode (E-Low).

The current consumption of XT1 oscillation circuit is equal to the harmony of DC bias current (I_{ds}^{*5}) and C_d charge current (I_d^{*6}).

The load capacitance of the circuit C_L ,

$$C_L = C_{ext} + C_s = C_g \times C_d / (C_g + C_d) + C_s \text{ (pF)}$$

where C_s stands for stray capacitance of the circuit.

Correlations between the oscillation mode selection of XT1 oscillation circuit and the recommended load capacitance for a resonator are shown in Table 1 for safety use.

SSP-T7 series

SSP-T7-FL $C_L=3.0pF, 3.7pF, 4.4pF, 6.0pF$ SSP-T7-F $C_L=7.0pF, 9.0pF$

$$I_{sub} = I_{ds} + I_d \text{ (}\mu A\text{)}$$

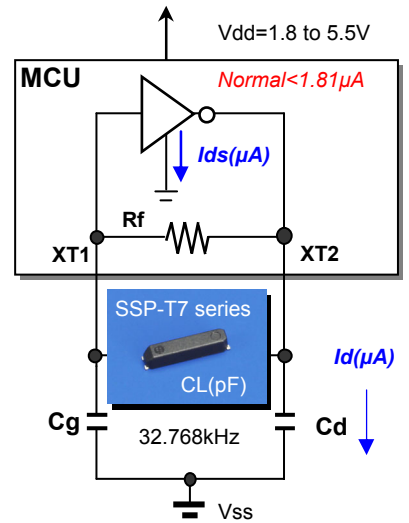
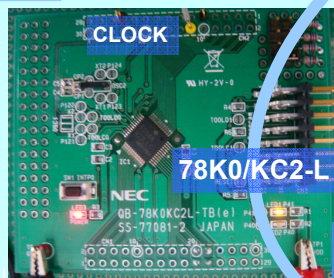
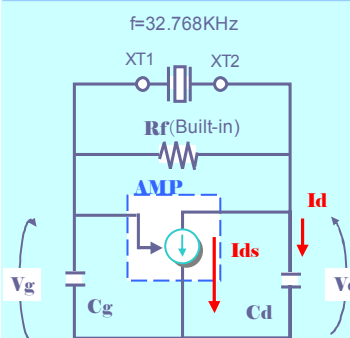


Table 1 Oscillation mode selection of XT1 oscillation circuit and load capacitance for a resonator

XT1 oscillation mode selection	Recommended circuit constant and load capacitance for a resonator				
	SSP-T7-FL 3.7pF	SSP-T7-FL 4.4pF	SSP-T7-FL 6.0pF	SSP-T7-F 7.0pF	SSP-T7-F 9.0pF
E-Low $I_{ds}=0.178\mu A$ $C_s=1.69pF$	$C_g=4.0pF, C_d=4.0pF$ $I_d=0.085\mu A$ typ $R_L=-920k\Omega$ typ $T_s=0.90sec$ typ	$C_g=6.0pF, C_d=5.0pF$ $I_d=0.102\mu A$ typ $R_L=-635k\Omega$ typ $T_s=1.09sec$ typ	$C_g=9.0pF, C_d=8.0pF$ $I_d=0.122\mu A$ typ $R_L=-354k\Omega$ typ $T_s=1.57sec$ typ	<i>Not recommended.</i>	<i>Not recommended.</i>
Low $I_{ds}=0.457\mu A$ $C_s=1.67pF$	<i>Not recommended.</i>	$C_g=6.0pF, C_d=5.0pF$ $I_d=0.177\mu A$ typ $R_L=-1027k\Omega$ typ $T_s=0.80sec$ typ	$C_g=9.0pF, C_d=8.0pF$ $I_d=0.219\mu A$ typ $R_L=-576k\Omega$ typ $T_s=1.11sec$ typ	$C_g=11pF, C_d=11pF$ $I_d=0.242\mu A$ typ $R_L=-389k\Omega$ typ $T_s=1.51sec$ typ	<i>Not recommended.</i>
Normal $I_{ds}=1.176\mu A$ $C_s=1.61pF$	<i>Not recommended.</i>	<i>Not recommended.</i>	$C_g=9.0pF, C_d=8.0pF$ $I_d=0.370\mu A$ typ $R_L=-925k\Omega$ typ $T_s=0.80sec$ typ	$C_g=11pF, C_d=11pF$ $I_d=0.421\mu A$ typ $R_L=-638k\Omega$ typ $T_s=0.92sec$ typ	$C_g=15pF, C_d=15pF$ $I_d=0.500\mu A$ typ $R_L=-388k\Omega$ typ $T_s=1.34sec$ typ

NEC MCU 78K0/KC2-L

- uPD78F0581GA, uPD78F0581GB
- uPD78F0582GA, uPD78F0582GB
- uPD78F0583GA, uPD78F0583GB
- uPD78F0586GA, uPD78F0586GB
- uPD78F0587GA, uPD78F0587GB
- uPD78F0588GA, uPD78F0588GB



The stray capacitance of the test board is C_s (1.60pF to 1.70pF).

*5; $I_{ds} = g_m (V_g - V_{TH}) / 2 = R_L (4\pi f C_L)^2 (V_g - V_{TH}) / 2$

*6; $I_d = 2\pi f C_d V_d = (4\pi f C_L) V_d$



Normal oscillation mode
 $I_{sub}=1.547\mu A, R_L=-925k\Omega$ at $C_L=6.0pF$

Normal current consumption < 1.81μA

Current consumption of the XT1 oscillation circuit I_{sub} ,
 $I_{sub} = I_{ds} + I_d \text{ (}\mu A\text{)}$



Normal oscillation mode
 $I_{sub}=1.597\mu A, R_L=-638k\Omega$ at $C_L=7.0pF$



Normal oscillation mode
 $I_{sub}=1.677\mu A, R_L=-388k\Omega$ at $C_L=9.0pF$