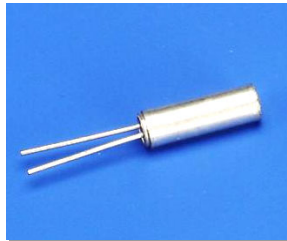


# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0148HGC-8BT] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V , 3.3V

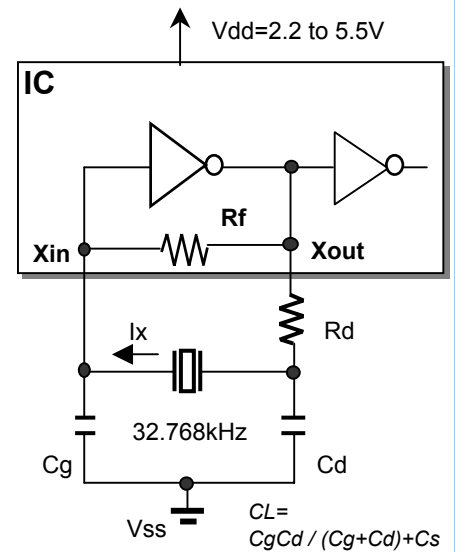
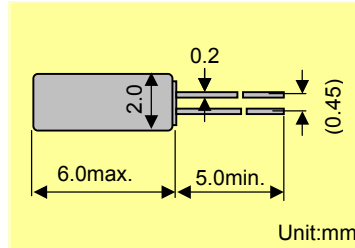


Model :VT-200  
 Frequency :Fo=32.768kHz  
 Frequency tolerance :dF/Fo= +/-20x10<sup>-6</sup>  
 Load capacitance :CL=6.0pF  
 Equivalent series resistance :R1=50kohm max  
 Max. Drive level :DL=x10<sup>-6</sup>W max  
 Recommended drive level :DL=0.1x10<sup>-6</sup>W typ

## FEATURES

- 1.Compact tubular package
- 2.Photolithographic process
- 3.Excellent shock resistance and environmental characteristics.
- 4.Real time clocks, Timers, Portable applications

## DIMENSIONS(VT-200)



Remark) Ix : current through crystal

MODEL:VT-200 6.0pF with uPD78F0148HGC at 25°C

Key specifications	Vdd=3.3V	Vdd=5.0V	Remarks
Current control resistance : Rd ( k ohm )	220	220	Control drive level & secure phase margin
Capacitance at gate : Cg ( pF )	6	8	Optimal capacity in response to CL
Capacitance at drain : Cd ( pF )	6	8	( CL = Cd // Cg + stray capacitance )

Circuit characteristics ( at 25°C )	Vdd=3.3V	Vdd=5.0V	Remarks
Matching Accuracy : df / f ( x10 <sup>-6</sup> )	-0.3	0.2	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V ( x10 <sup>-6</sup> )	6.6	6.7	Vdd +/-10% ( Standard operating voltage range )
Drive Level : DL ( x10 <sup>-6</sup> W )	0.03	0.05	DL=Ix <sup>2</sup> Re < 1x10 <sup>-6</sup> W, Re=R1( 1 + Co / CL ) <sup>2</sup>
Negative resistance :   - RL   ( kohm )	599	549	5 times larger than R <sub>1MAX</sub>
Oscillation allowance : M ( times )	12.0	11.0	Judgemental standard of oscillation stability
Oscillation start up time : Ts ( sec )	0.80	0.80	Time to reach 90% of output level

Temperature characteristics of circuit	Vdd=3.3V	Vdd=5.0V	Remarks
at -40°C Variation : df / T ( x10 <sup>-6</sup> )	-135	-134	Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> )
at +85°C Variation : df / T ( x10 <sup>-6</sup> )	-136	-136	Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> )

The mention value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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We value the "takumi" spirit.

Seiko Instruments Inc.

Phone:+81-43-211-1207(Direct)

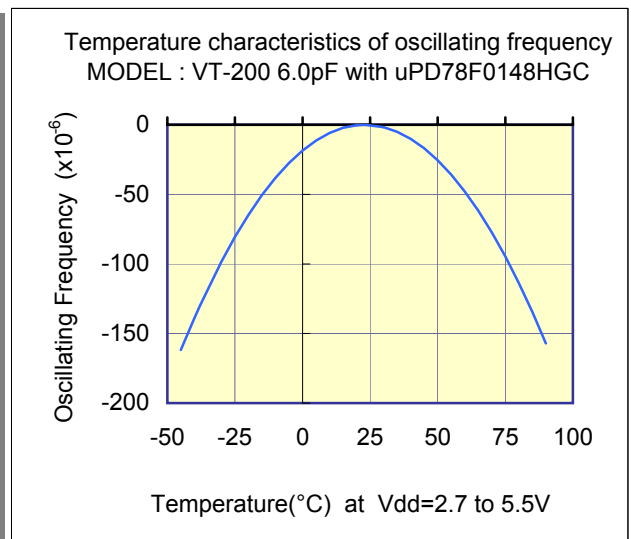
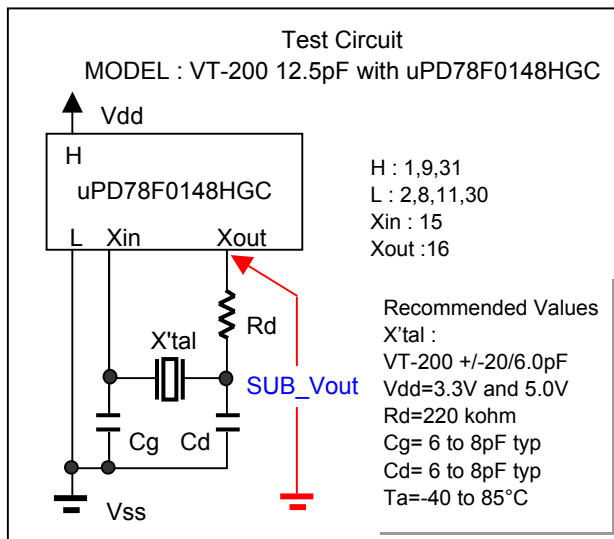
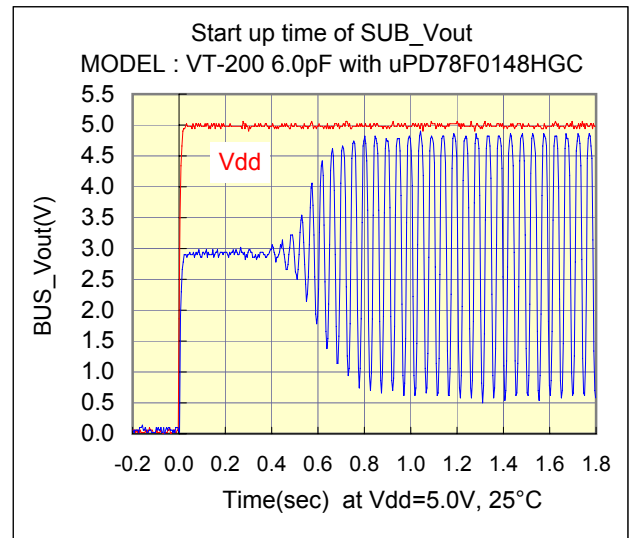
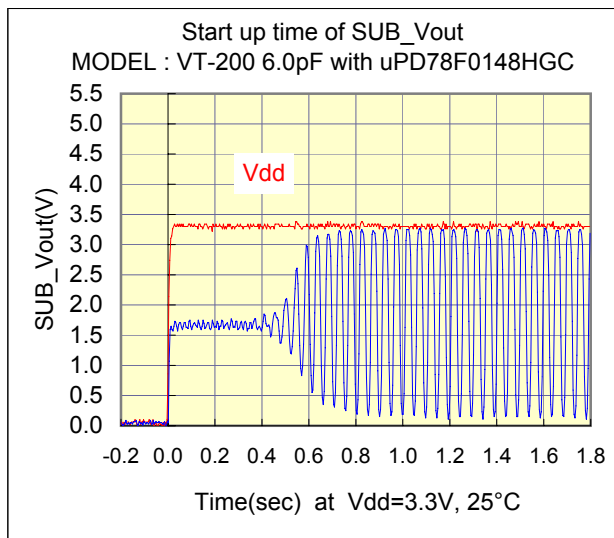
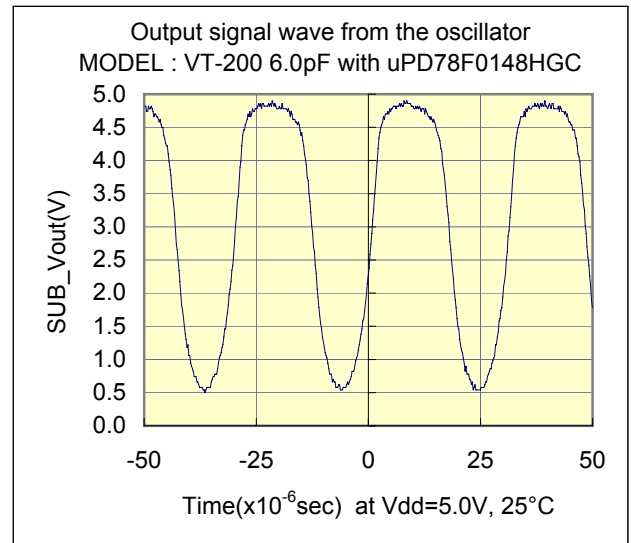
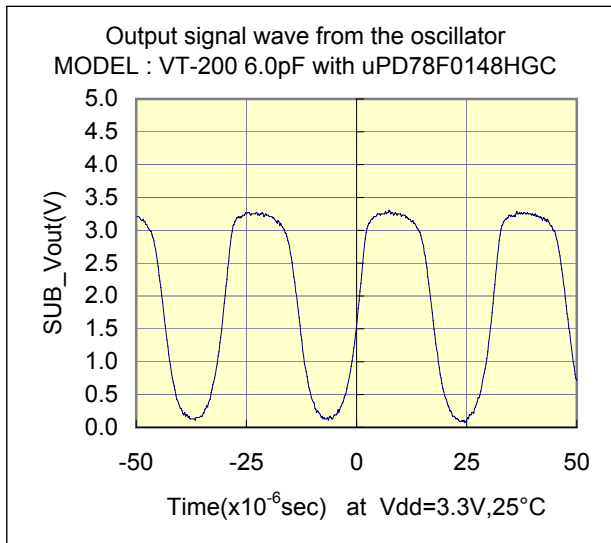
# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0148HGC] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V , 3.3V



## Test Data



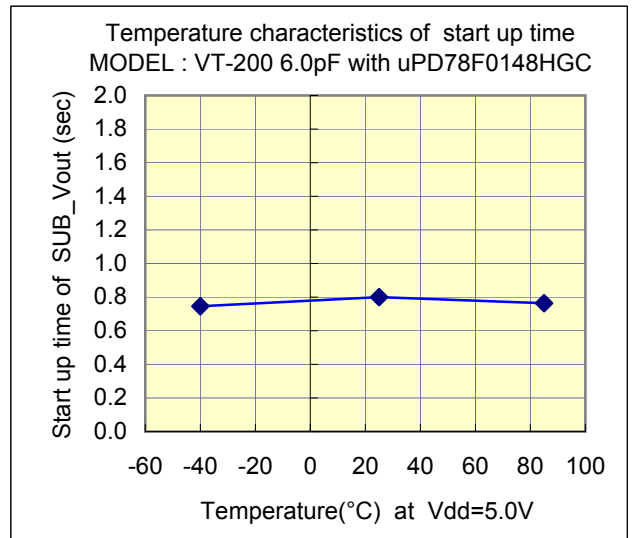
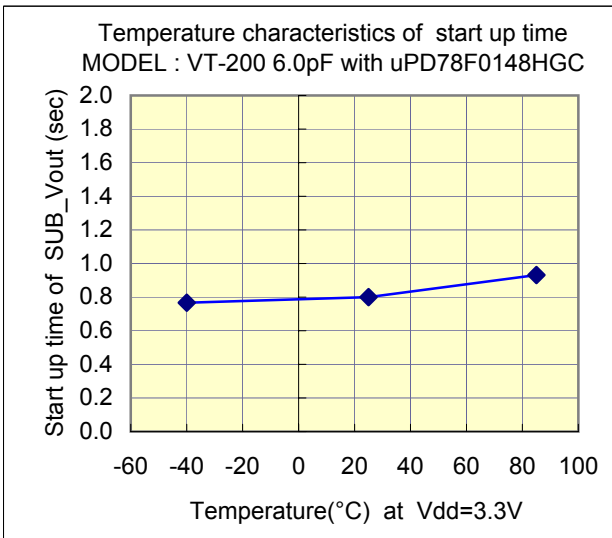
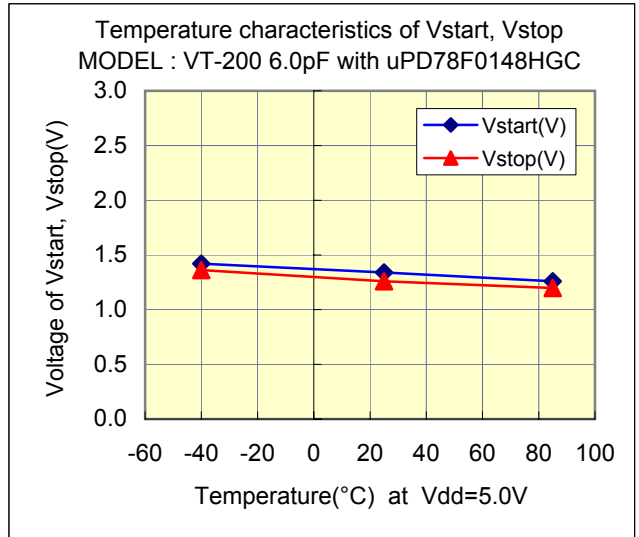
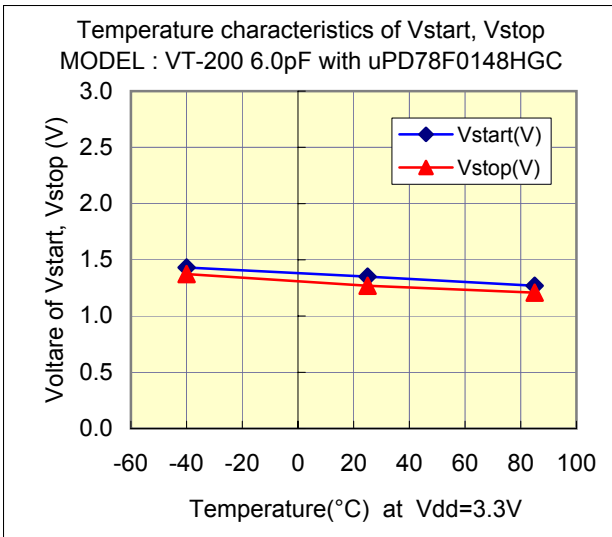
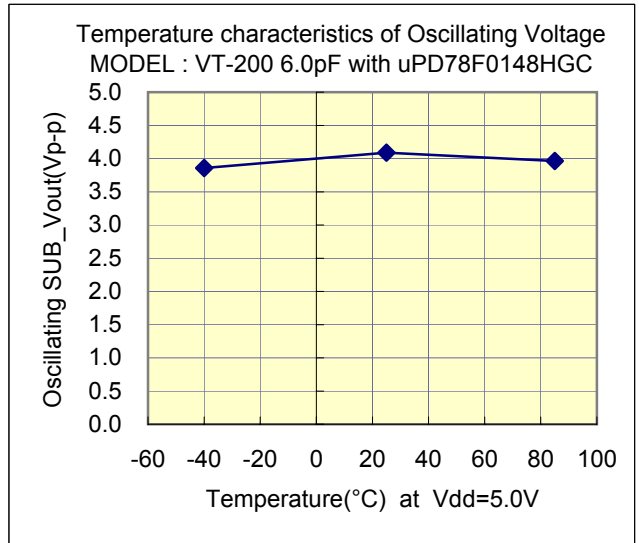
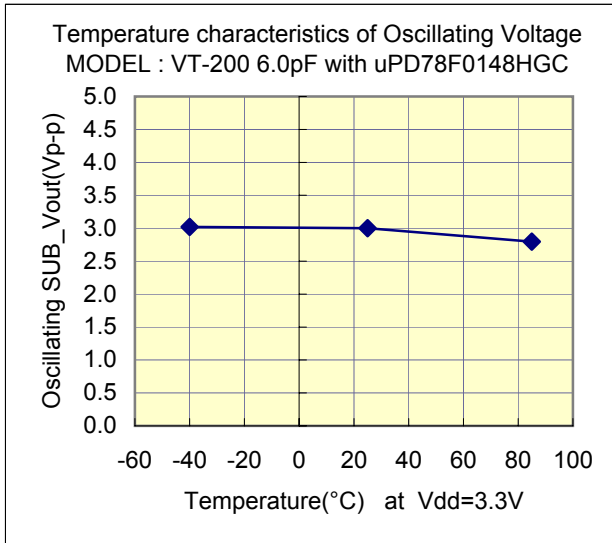
# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0148HGC-8BT] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V , 3.3V



## Test Data : Temperature characteristics

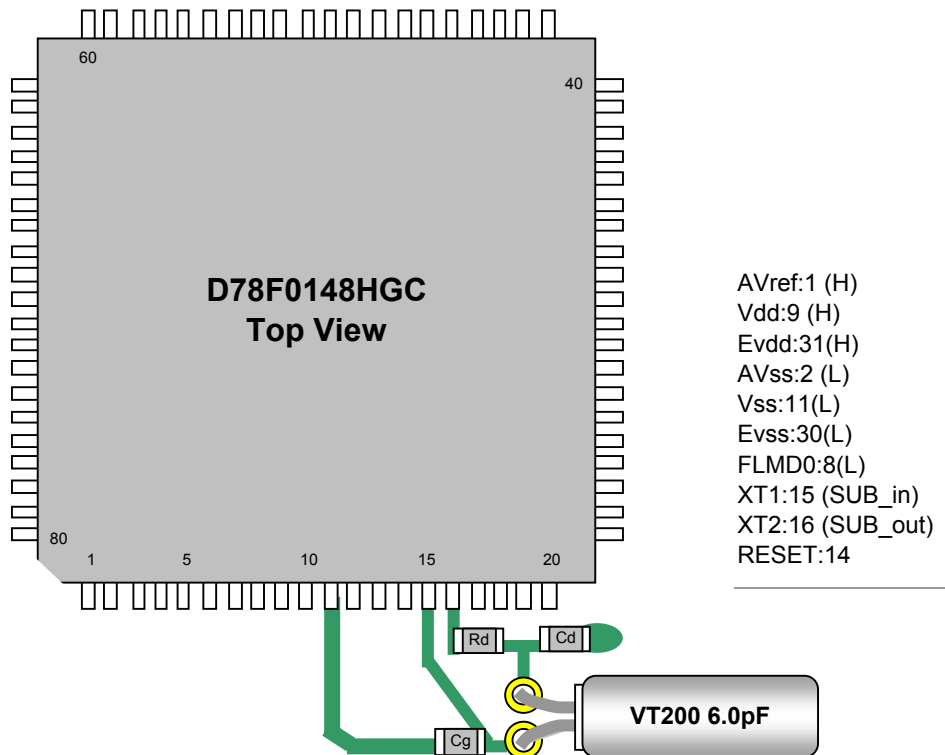


# Evaluation of Subsystem Clock Oscillation Circuit

[ $\mu$ PD78F0148HGC-8BT] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V , 3.3V

## Referencial components layout(see Figure 1)

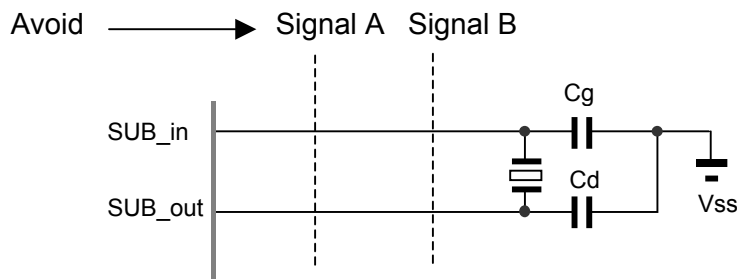


**Figure 1 Referencial components layout**

## Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB\_in and SUB\_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).



**Figure 2 Example of Incorrect Board Design**

**Remak** When using the subsystem clock, insert resistors Rd in series on the SUB\_out side.

# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0148HGC-8BT] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V , 3.3V

## [Evaluation Sample : VT-200 6.0pF at 25°C]

SAMPLE	No.	CL( pF )	Fo( Hz )	fr( Hz )	R1( kohm )	Co( pF )	C1( fF )	Q( k )
VT-200 6.0pF	1	6	32768.18	32762.98	28.7	0.91	2.193	77.2
	2	6	32768.18	32763.04	27.8	0.89	2.161	80.9
	3	6	32768.19	32763.00	27.2	0.90	2.187	81.7

## [IC Test Data : IC Sampl Rd=220 ohm,Cg=8pF,Cd=8pF at 25°C]

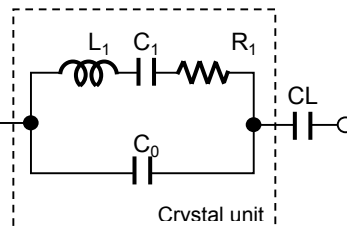
Vcc( V )	IC Sampl	Fosc( Hz )	df / f( x10 <sup>-6</sup> )	DL(x10 <sup>-6</sup> W)	-RL  ( kohm )	Vstart( V )	Ts(sec)
5.0	HHH500	32768.19	0.15	0.05	549	1.34	0.80
	LLL500	32768.18	0.00	0.03	549	1.09	0.80

## [IC Test Data : IC Sampl Rd=220 ohm,Cg=6pF,Cd=6pF at 25°C]

Vcc( V )	IC Sampl	Fosc( Hz )	df / f( x10 <sup>-6</sup> )	DL(x10 <sup>-6</sup> W)	-RL  ( kohm )	Vstart( V )	Ts(sec)
3.3	HHH500	32768.17	-0.31	0.03	599	1.35	0.80
	LLL500	32768.24	1.83	0.02	599	1.11	0.80

### Remak ( see figure 3 )

$$F_o = f_r \times \left\{ \frac{C_1}{2 \times (C_o + C_L)} + 1 \right\} \text{ ( Hz )}$$



Fo : Load resonance frequency  
 fr : Resonance frequency  
 R1 : Motional resistance  
 C1 : Motional capacitance  
 Co : Shunt capacitance  
 CL : Load Capacitance

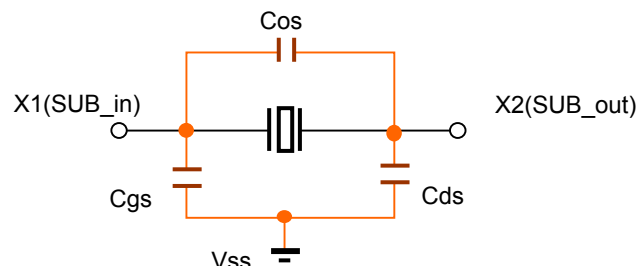
Figure 3 Equivalent circuit of crystal unit, and CL

### Remak ( see figure 4 )

Approximate formula of the load capacitance of the circuit CL.

$$CL = C_g \times C_d / (C_g + C_d) + C_s \text{ ( pF )}$$

Where Cs Stands for stray capacity of the circuit.



Cos : X1\_X2 Stray capacitance  
 Cgs : X1\_Vss Stray capacitance  
 Cds : X2\_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.