

# Evaluation of Subsystem Clock Oscillation Circuit

[HD64F36049GH-80A] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V (in use of regulator), 3.3V (non use of regulator)

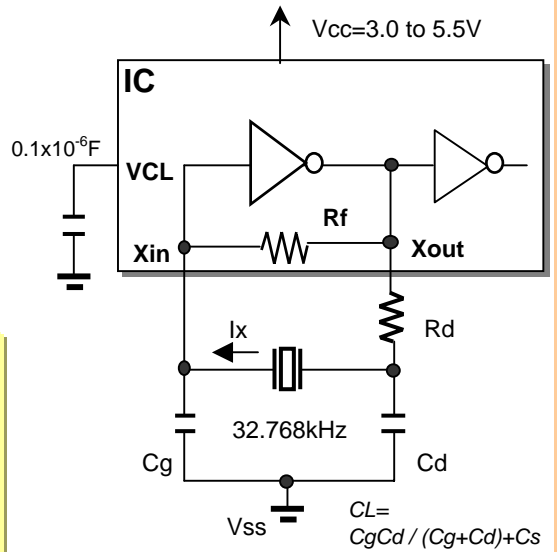
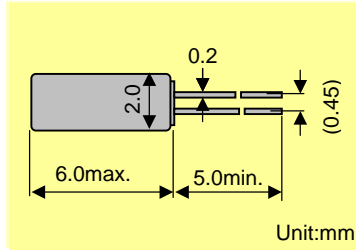


Model :VT-200  
 Frequency :Fo=32.768kHz  
 Frequency tolerance :dF/Fo= +/-20x10<sup>-6</sup>  
 Load capacitance :CL=12.5pF  
 Equivalent series resistance :R1=50kohm max  
 Max. Drive level :DL=x10<sup>-6</sup>W max  
 Recommended drive level :DL=0.1x10<sup>-6</sup>W typ

### FEATURES

- 1.Compact tubular package
- 2.Photolithographic process
- 3.Excellent shock resistance and environmental characteristics.
- 4.Real time clocks, Timers, Portable applications

### DIMENSIONS(VT-200)



Remark) Ix : current through crystal

When the internal power supply Step-Down circuit is not used, please connect the external power supply to the VCL pin and Vcc pin.

The permissible range for the power supply voltage is 3.0V to 3.6V.

MODEL:VT-200 12.5pF with HD64F36049GH at 25°C

Key specifications	Vcc=3.3V	Vcc=5.0V	Remarks
Current control resistance : Rd ( k ohm )	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg ( pF )	18	18	Optimal capacity in response to CL
Capacitance at drain : Cd ( pF )	15	15	( CL = Cd // Cg + stray capacitance )

Circuit characteristics ( at 25°C )	Vcc=3.3V	Vcc=5.0V	Remarks
Matching Accuracy : df / f ( x10 <sup>-6</sup> )	-0.9	-0.6	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V ( x10 <sup>-6</sup> )	1.2	0.0	Vdd +/-10% ( Standard operating voltage range )
Drive Level : DL ( x10 <sup>-6</sup> W )	0.31	0.30	DL=Ix <sup>2</sup> Re < 1x10 <sup>-6</sup> W, Re=R1( 1 + Co / CL ) <sup>2</sup>
Negative resistance :   - RL   ( kohm )	594	544	5 times larger than R1MAX
Oscillation allowance : M ( times )	11.9	10.9	Judgemental standard of oscillation stability
Oscillation start up time : Ts ( sec )	0.83	0.75	Time to reach 90% of output level

Temperature characteristics of circuit	Vcc=3.3V	Vcc=5.0V	Remarks
at -40°C Variation : df / T ( x10 <sup>-6</sup> )	-143	-143	Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> )
at +85°C Variation : df / T ( x10 <sup>-6</sup> )	-125	-125	Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> )

The mention value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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We value the "takumi" spirit.

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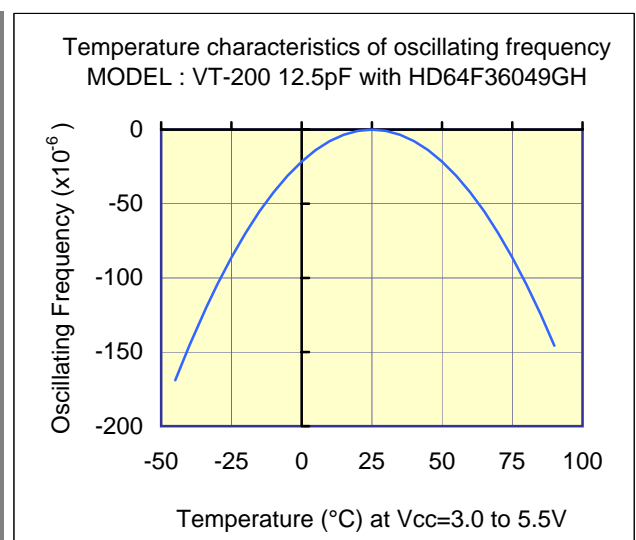
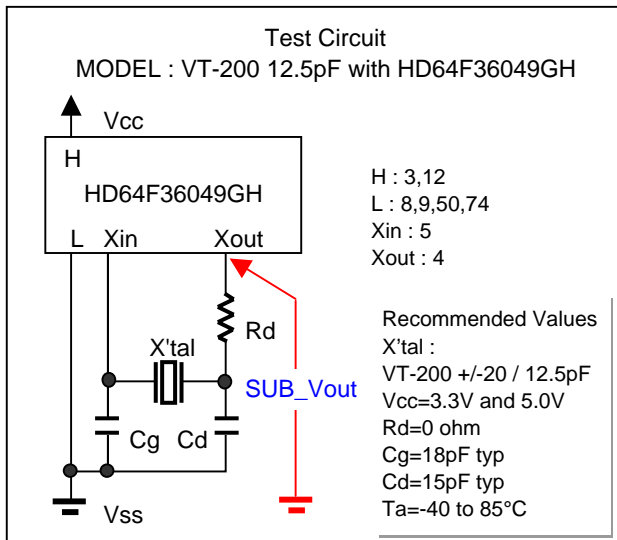
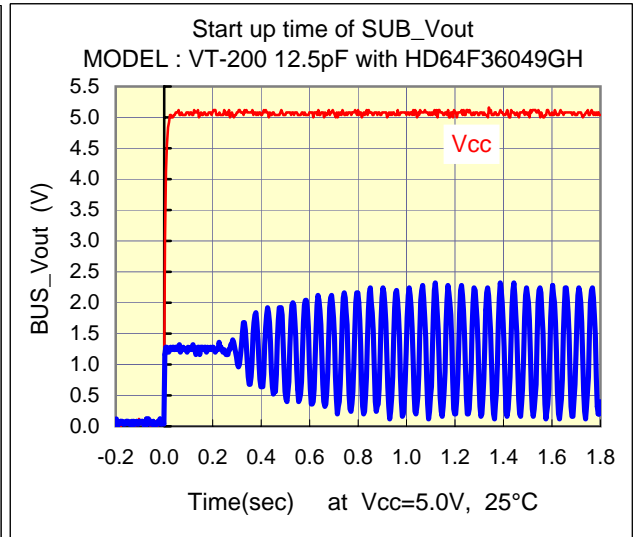
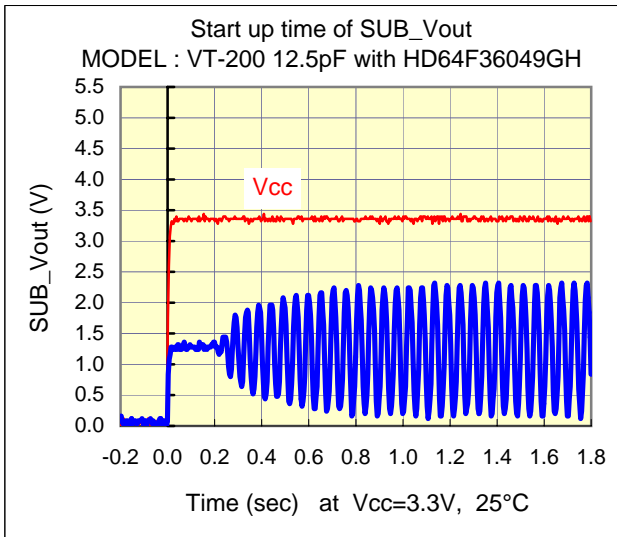
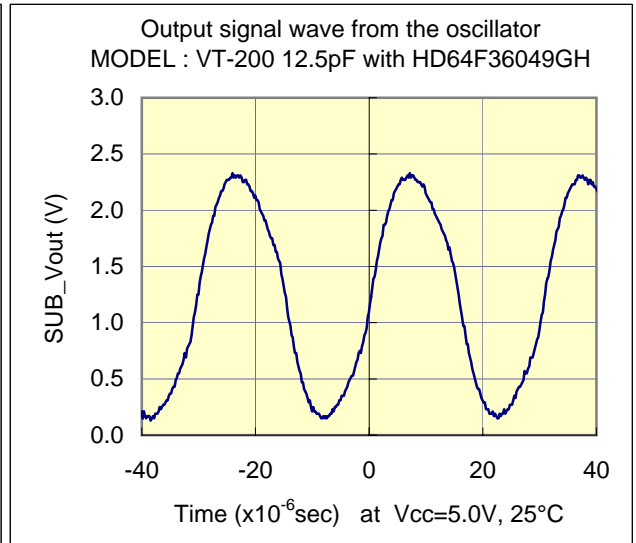
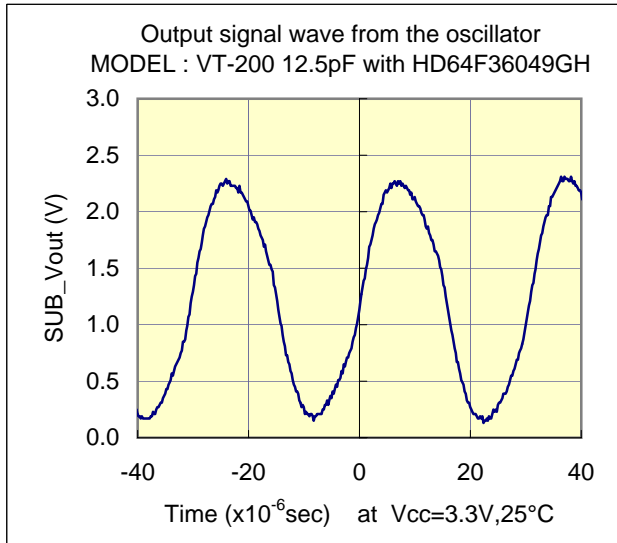
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## Test Data



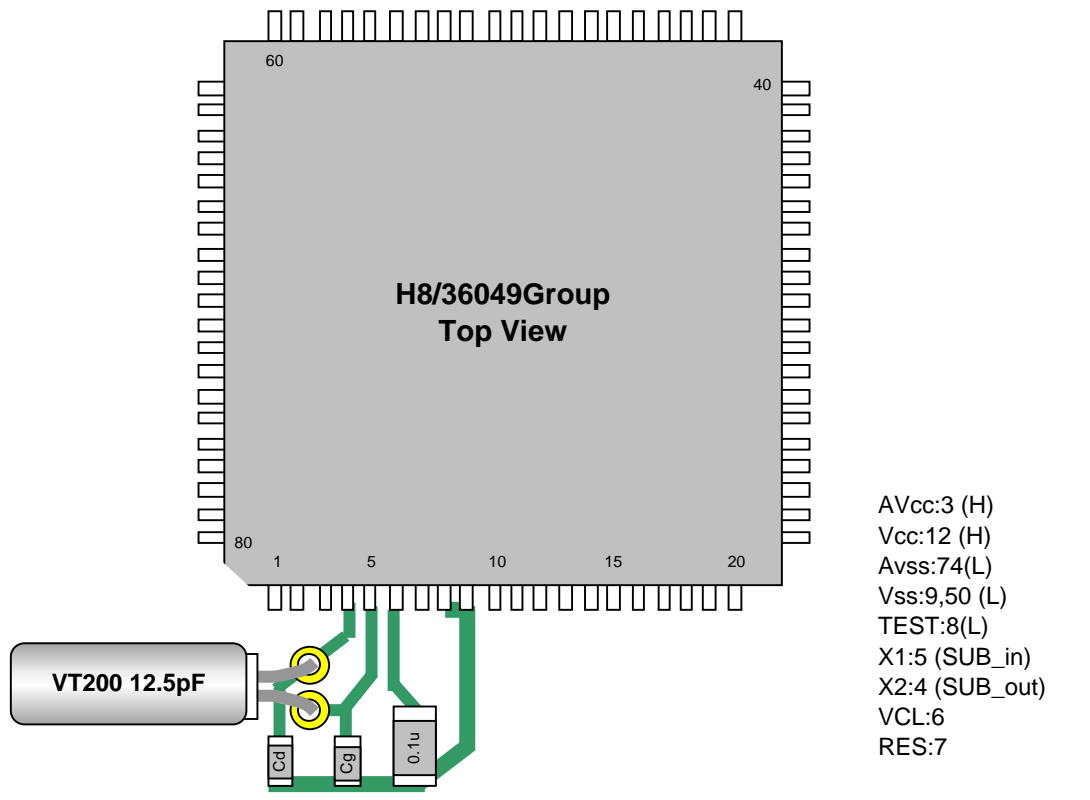
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## Referencial components layout ( see Figure 1 )

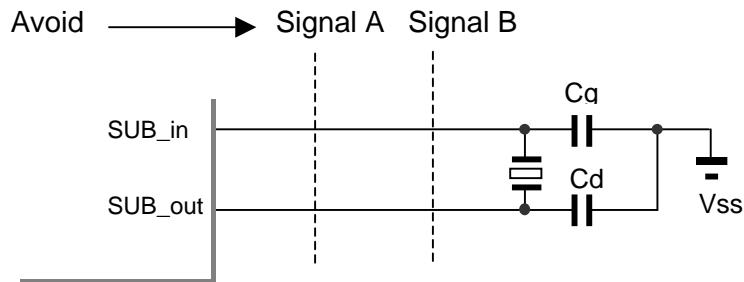


**Figure 1 Referencial components layout**

### Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB\_in and SUB\_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).



**Figure 2 Example of Incorrect Board Design**

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## [Evaluation Sample : VT-200 12.5pF at 25°C]

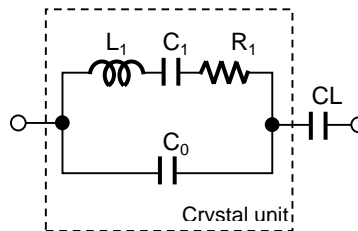
SAMPLE	No.	CL( pF )	Fo( Hz )	fr( Hz )	R1( kohm )	Co( pF )	C1( fF )	Q( k )
VT-200 12.5pF	1	12.5	32768.11	32765.28	27.4	0.91	2.319	76.5
	2	12.5	32768.09	32765.24	26.9	0.89	2.333	77.4
	3	12.5	32768.37	32765.47	28.8	0.92	2.372	71.1

## [IC Test Data : IC samples Rd=0 ohm,Cg=18pF,Cd=15pF at 25°C]

Vcc( V )	IC typ	Fosc( Hz )	df / f( x10 <sup>-6</sup> )	DL(x10 <sup>-6</sup> W)	-RL  (kohm)	Vstart( V )	Ts(sec)
5.0	Typ	32768.32	-0.6	0.30	544	1.22	0.75
	N_high/P_low	32768.36	0.6	0.31	594	1.14	0.74
	N_low/P_high	32768.35	0.3	0.33	594	1.36	0.76
3.3	Typ	32768.31	-0.9	0.31	594	1.54	0.83
	N_high/P_low	32768.34	0.0	0.32	594	1.14	0.76
	N_low/P_high	32768.33	-0.3	0.32	594	1.36	0.79

### Remak ( see figure 3 )

$$F_o = f_r \times \left\{ \frac{C_1}{2 \times (C_o + C_L)} + 1 \right\} \text{ ( Hz )}$$



- Fo : Load resonance frequency
- fr : Resonance frequency
- R1 : Motional resistance
- C1 : Motional capacitance
- Co : Shunt capacitance
- CL : Load Capacitance

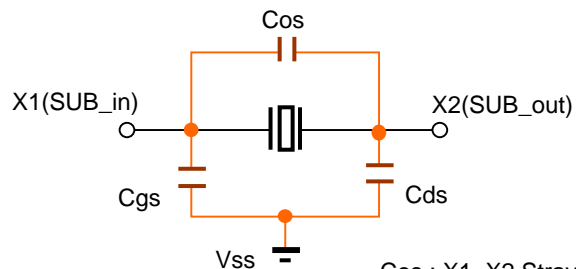
Figure 3 Equivalent circuit of crystal unit, and CL

### Remak ( see figure 4 )

Approximate formula of the load capacitance of the circuit CL.

$$CL = C_g \times C_d / (C_g + C_d) + C_s \text{ (pF)}$$

Where Cs Stands for stray capacity of the circuit.



- Cos : X1\_X2 Stray capacitance
- Cgs : X1\_Vss Stray capacitance
- Cds : X2\_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.