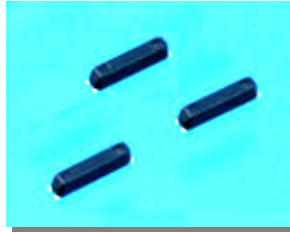


Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0148HGC-8BT] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V , 3.3V

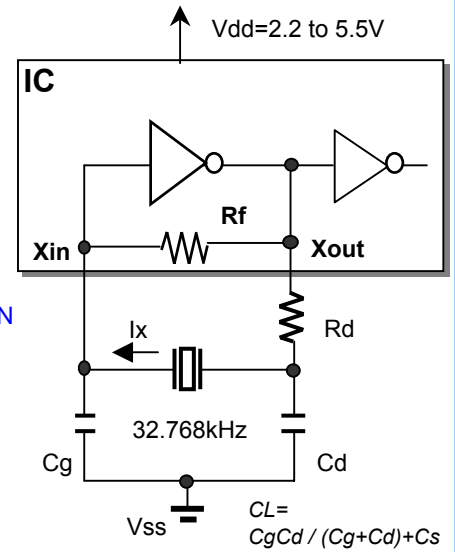
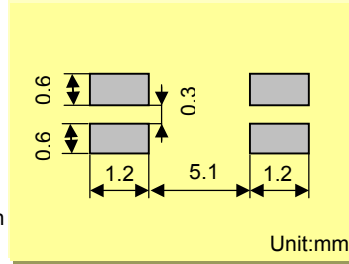


Model :SSP-T7
 Frequency :Fo=32.768kHz
 Frequency tolerance :dF/Fo= +/-20x10⁻⁶
 Load capacitance :CL=12.5pF
 Equivalent series resistance :R1=65kohm max
 Max. Drive level :DL=x10⁻⁶W max
 Recommended drive level :DL=0.1x10⁻⁶W typ

FEATURES

- 1.Ultra thin type with 1.4mm Max.
- 2.SMD type suitable for automatic & high density surface mounting.
- 3.Plastic mold package containing highly reliable tubular type quartz crystal.
- 4.Excellent shock and heat resistance.
- 5.Cellular phones,PDA,Radio communication equipment, Portable applications etc.

RECOMMENDED SOLDERIN PATTERN



Remark) I_x : current through crystal

MODEL:SSP-T7 12.5pF with uPD78F0148HGC at 25°C

Key specifications	Vdd=3.3V	Vdd=5.0V	Remarks
Current control resistance : Rd (k ohm)	220	220	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	18	20	Optimal capacity in response to CL
Capacitance at drain : Cd (pF)	18	18	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vdd=3.3V	Vdd=5.0V	Remarks
Matching Accuracy : df / f ($\times 10^{-6}$)	-0.3	3.7	Frequency offset volume at specified Vdd
Voltage Fluctuation : $\pm df / V$ ($\times 10^{-6}$)	1.5	1.8	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL ($\times 10^{-6}$ W)	0.39	0.53	$DL = I_x^2 R_e < 1 \times 10^{-6} W, R_e = R_1 (1 + C_o / CL)^2$
Negative resistance : $ -RL $ (kohm)	407	517	5 times larger than R_{1MAX}
Oscillation allowance : M (times)	6.3	8.0	Judgemental standard of oscillation stability
Oscillation start up time : Ts (sec)	1.05	0.95	Time to reach 90% of output level

Temperature characteristics of circuit	Vdd=3.3V	Vdd=5.0V	Remarks
at -40°C Variation : df / T ($\times 10^{-6}$)	-139	-139	Typ.Tp=25°C (K = $-3.5 \times 10^{-8} / ^\circ C^2$)
at +85°C Variation : df / T ($\times 10^{-6}$)	-123	-124	Typ.Tp=25°C (K = $-3.5 \times 10^{-8} / ^\circ C^2$)

The mention value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

Seiko Instruments USA Inc.

2990,West Lomita Blvd., Torrance, CA 90505, U.S.A

Telephone :+1 310-517-7771 Facsimile :+1 310-517-7792

Email :crystals@siu-la.com

Seiko Instruments GmbH

Siemensstrasse 9,D-63263 Neu-Isenburg,Germany

Telephone :+49-6102-297-0 Facsimile :+49-6102-297-320

Email :info@seiko-instruments.de

Seiko Instruments Inc.

1-8,Nakase,Mihama-ku,Chiba-shi,Chiba 261-8507,Japan

Facsimile :+81-43-211-8030 E-mail :component@sii.co.jp



We value the "takumi" spirit.

Seiko Instruments Inc.

Phone:+81-43-211-1207(Direct)

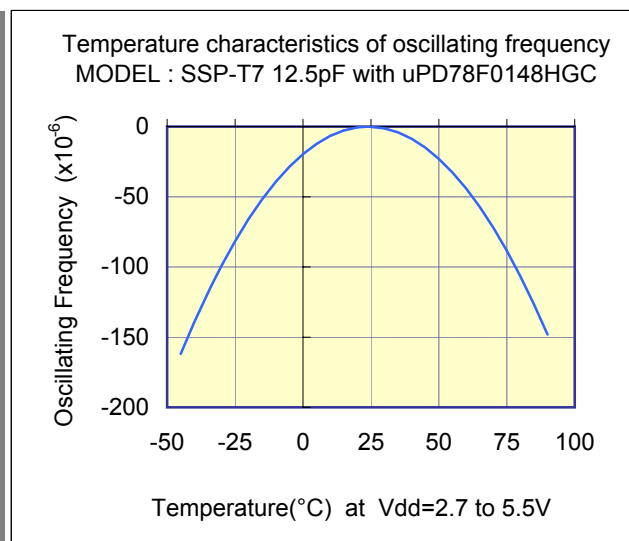
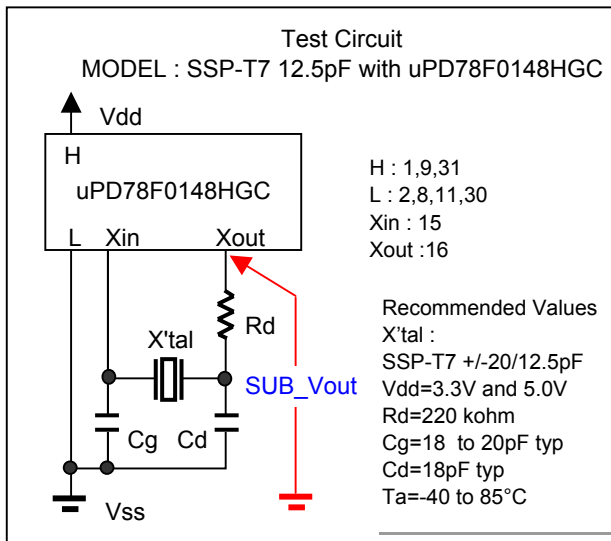
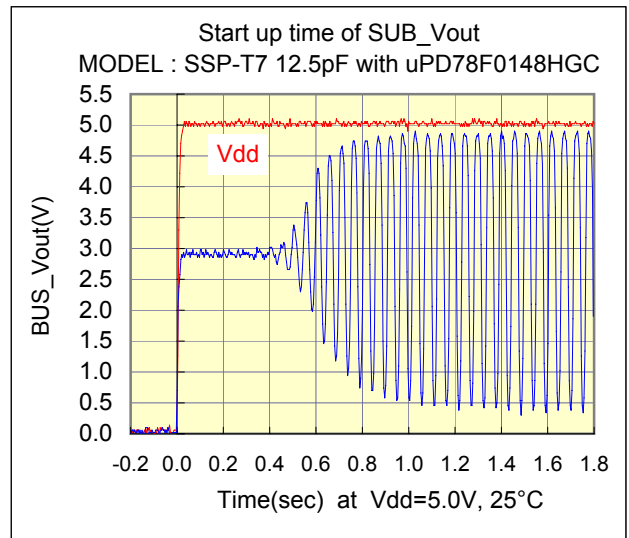
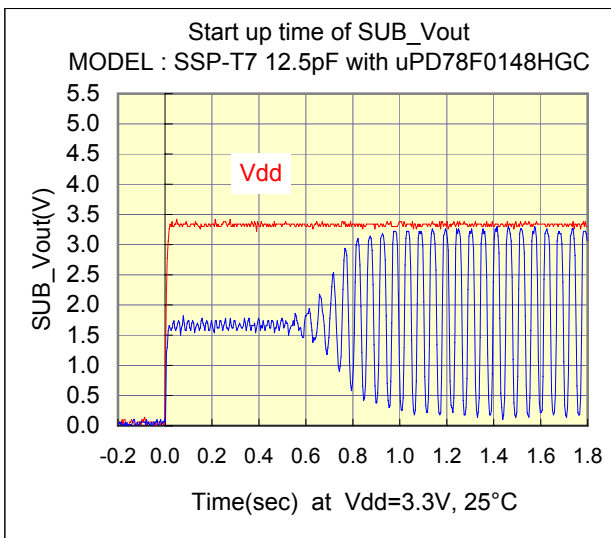
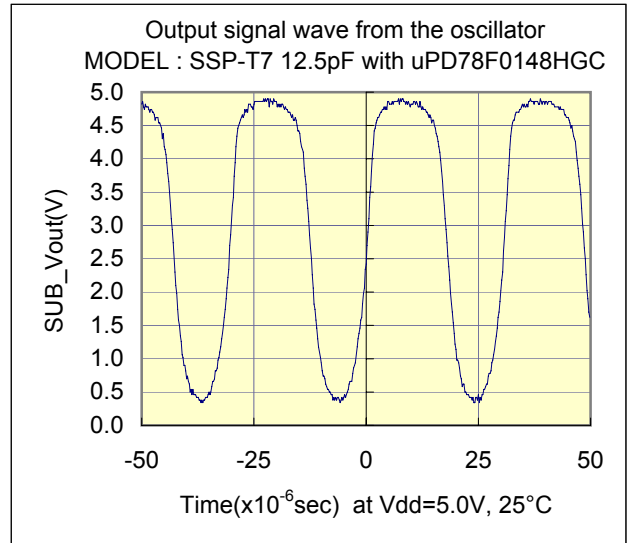
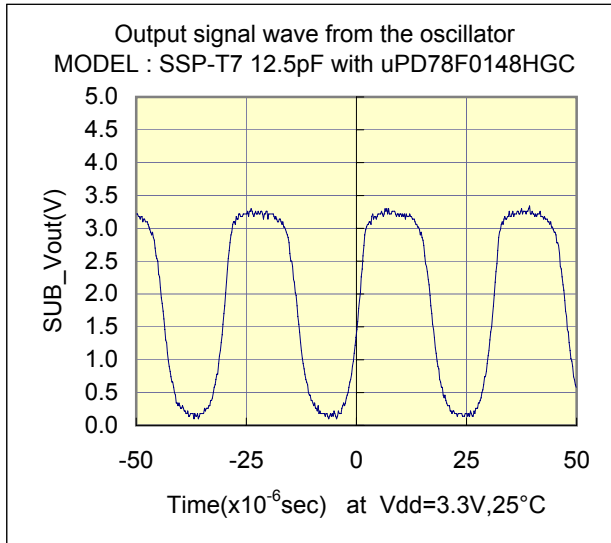
Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0148HGC] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V , 3.3V



Test Data



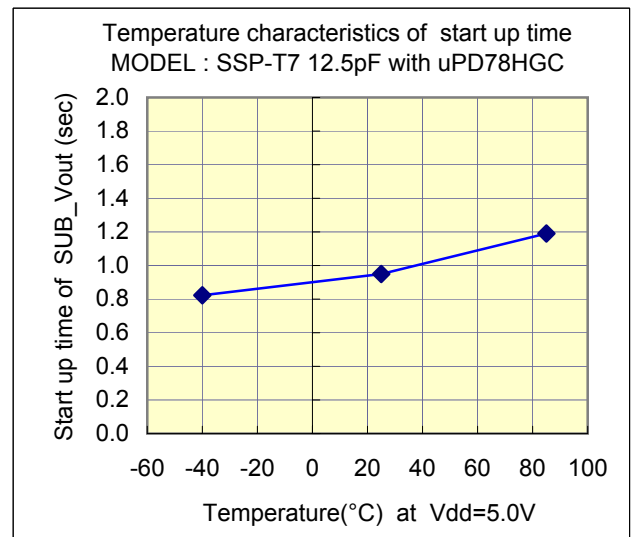
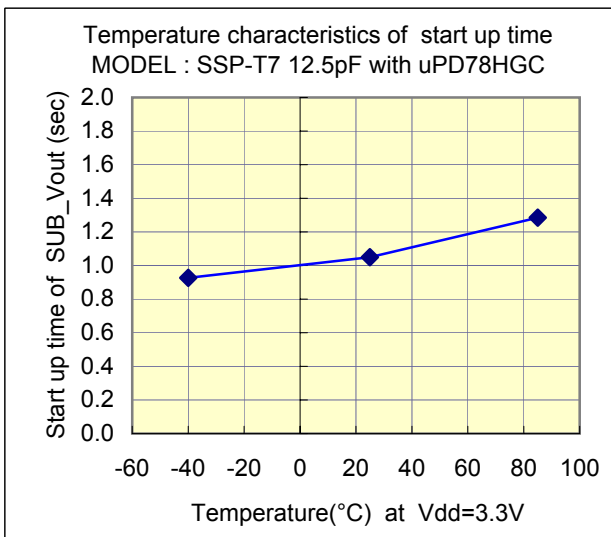
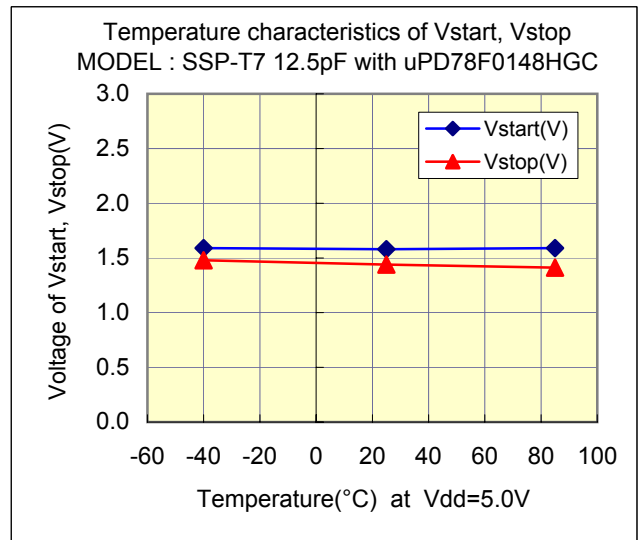
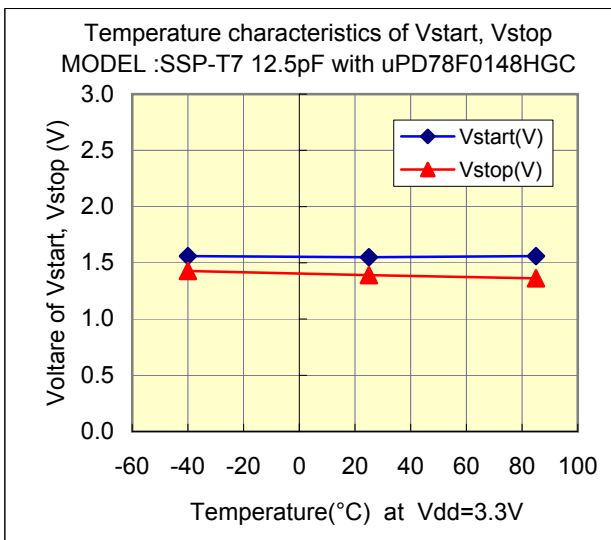
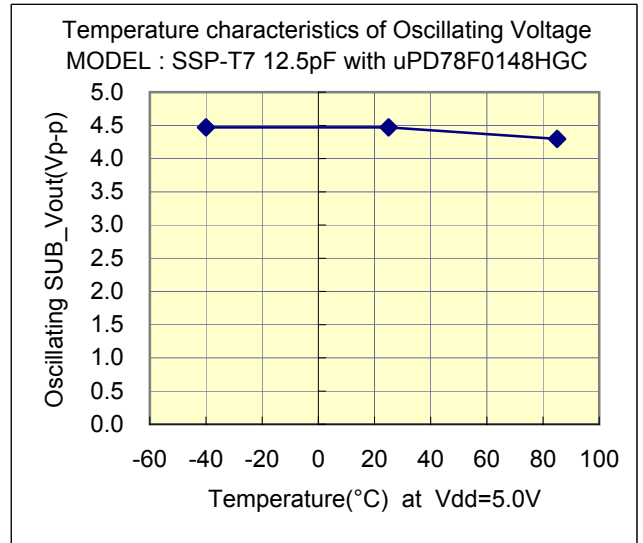
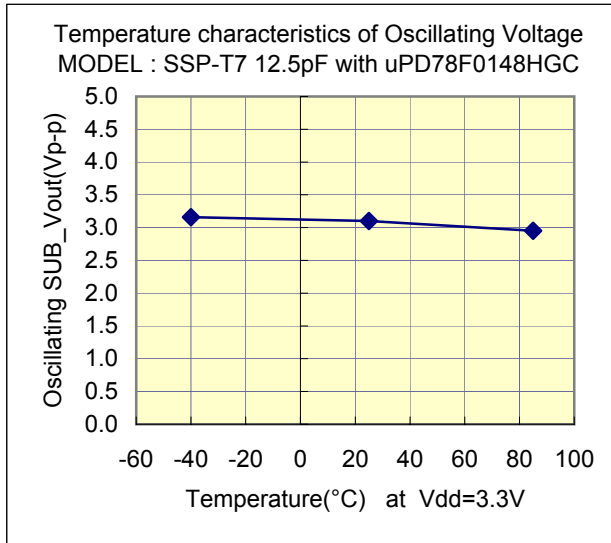
Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0148HGC-8BT] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V , 3.3V



Test Data : Temperature characteristics



Evaluation of Subsystem Clock Oscillation Circuit

[μ PD78F0148HGC-8BT] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V , 3.3V

Referencial components layout(see Figure 1)

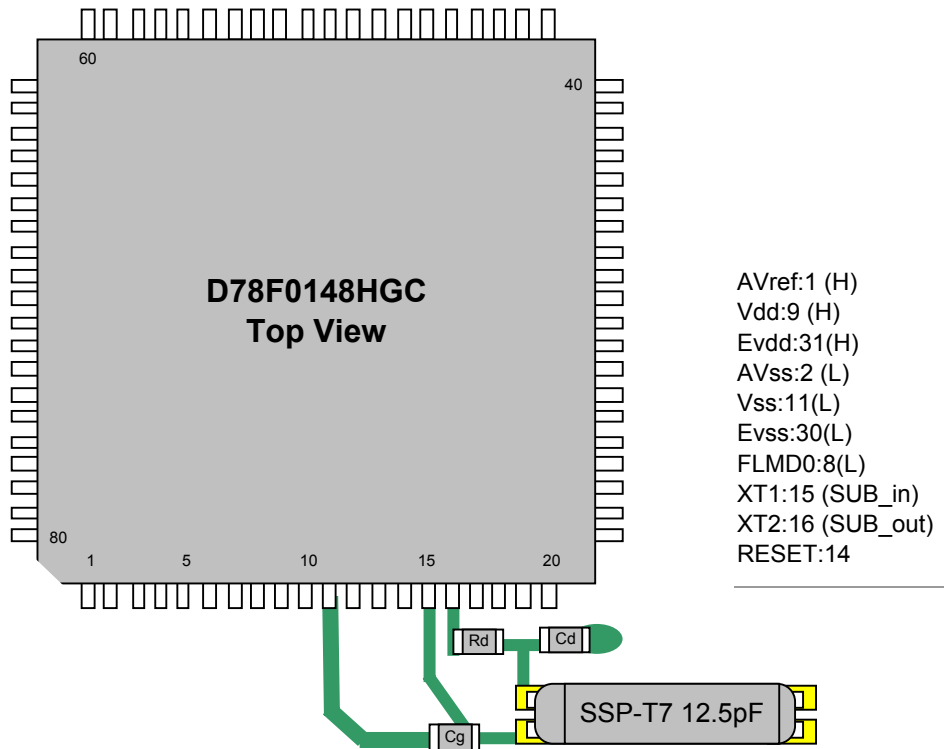


Figure 1 Referencial components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

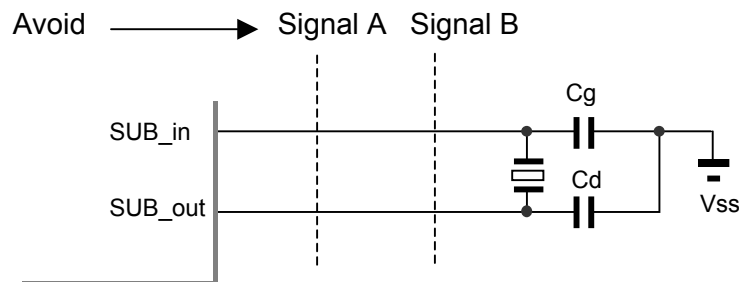


Figure 2 Example of Incorrect Board Design

Remak When using the subsystem clock, insert resistors Rd in series on the SUB_out side.

Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0148HGC-8BT] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V , 3.3V

[Evaluation Sample : SSP-T7 12.5pF at 25°C]

SAMPLE	No.	CL (pF)	Fo (Hz)	fr (Hz)	R1 (kohm)	Co (pF)	C1 (fF)	Q (k)
SSP-T7 12.5pF	1	12.5	32768.24	32765.77	41.5	0.86	2.014	58.1
	2	12.5	32768.14	32765.66	38.0	0.88	2.025	63.2
	3	12.5	32768.06	32765.60	45.1	0.84	2.003	53.8

[IC Test Data : IC Sampl Rd=220 ohm,Cg=20pF,Cd=18pF at 25°C]

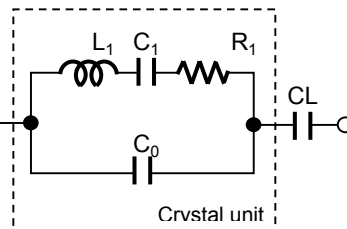
Vcc (V)	IC Sampl	Fosc (Hz)	df / f (x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart (V)	Ts(sec)
5.0	HHH500	32768.36	3.66	0.53	517	1.58	0.95
	LLL500	32768.40	4.88	0.39	517	1.25	0.95

[IC Test Data : IC Sampl Rd=220 ohm,Cg=18pF,Cd=18pF at 25°C]

Vcc (V)	IC Sampl	Fosc (Hz)	df / f (x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart (V)	Ts(sec)
3.3	HHH500	32768.23	-0.31	0.39	407	1.55	1.05
	LLL500	32768.29	1.53	0.29	437	1.23	0.98

Remak (see figure 3)

$$F_o = f_r \times \left\{ \frac{C_1}{2 \times (C_o + C_L)} + 1 \right\} \text{ (Hz)}$$



Fo : Load resonance frequency
 fr : Resonance frequency
 R1 : Motional resistance
 C1 : Motional capacitance
 Co : Shunt capacitance
 CL : Load Capacitance

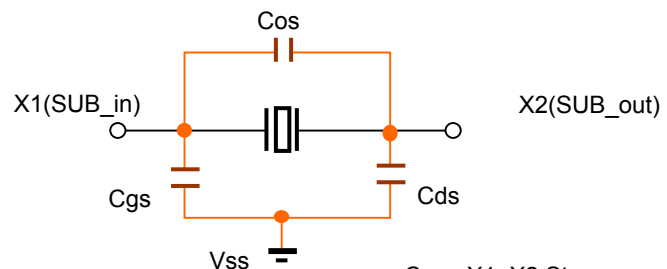
Figure 3 Equivalent circuit of crystal unit, and CL

Remak (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

$$CL = C_g \times C_d / (C_g + C_d) + C_s \text{ (pF)}$$

Where Cs Stands for stray capacity of the circuit.



Cos : X1_X2 Stray capacitance
 Cgs : X1_Vss Stray capacitance
 Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.