

Evaluation of Subsystem Clock Oscillation Circuit

[HD64336049GH-80A] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V (in use of regulator), 3.3V (non use of regulator)

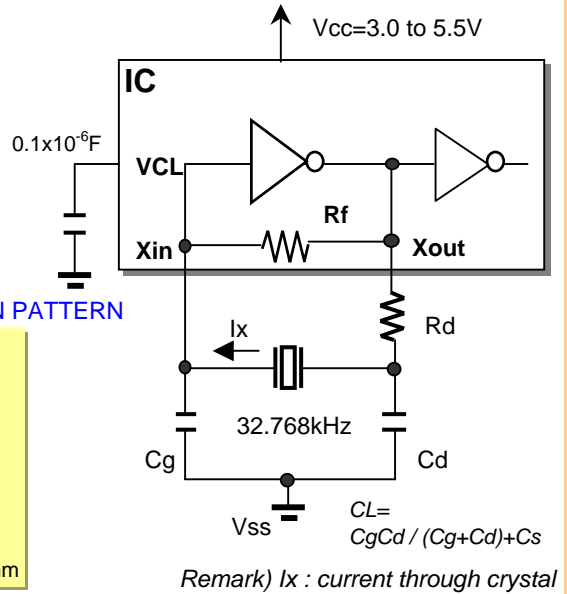
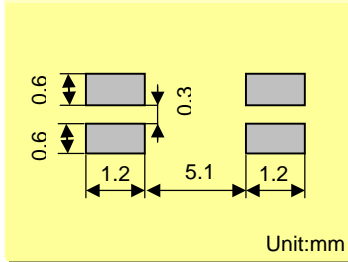


Model :SSP-T7
 Frequency :Fo=32.768kHz
 Frequency tolerance :dF/Fo= +/-20x10⁻⁶
 Load capacitance :CL=7.0pF
 Equivalent series resistance :R1=65kohm max
 Max. Drive level :DL=x10⁻⁶W max
 Recommended drive level :DL=0.1x10⁻⁶W typ

FEATURES

- 1.Ultra thin type with 1.4mm Max.
- 2.SMD type suitable for automatic & high density surface mounting.
- 3.Plastic mold package containing highly reliable tubular type quartz crystal.
- 4.Excellent shock and heat resistance.
- 5.Cellular phones,PDA,Radio communication equipment, Portable applications etc.

RECOMMENDED SOLDERIN PATTERN



When the internal power supply Step-Down circuit is not used, please connect the external power supply to the VCL pin and Vcc pin.

The permissible range for the power supply voltage is 3.0V to 3.6V.

MODEL:SSP-T7 7.0pF with HD64336049GH at 25°C

Key specifications	Vcc=3.3V	Vcc=5.0V	Remarks
Current control resistance : Rd (k ohm)	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	7	7	Optimal capacity in response to CL
Capacitance at drain : Cd (pF)	7	7	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vcc=3.3V	Vcc=5.0V	Remarks
Matching Accuracy : df / f (x10 ⁻⁶)	-3.1	-2.4	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V (x10 ⁻⁶)	1.8	0.0	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL (x10 ⁻⁶ W)	0.08	0.08	DL=Ix ² Re < 1x10 ⁻⁶ W, Re=R1(1 + Co / CL) ²
Negative resistance : - RL (kohm)	1047	1047	5 times larger than R1MAX
Oscillation allowance : M (times)	16.1	16.1	Judgemental standard of oscillation stability
Oscillation start up time : Ts (sec)	0.73	0.67	Time to reach 90% of output level

Temperature characteristics of circuit	Vcc=3.3V	Vcc=5.0V	Remarks
at -40°C Variation : df / T (x10 ⁻⁶)	-128	-128	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)
at +85°C Variation : df / T (x10 ⁻⁶)	-132	-132	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)

The mention value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

Seiko Instruments USA Inc.

2990,West Lomita Blvd., Torrance, CA 90505, U.S.A
 Telephone :+1 310-517-7771 Facsimile :+1 310-517-7792
 Email :crystals@siu-la.com

Seiko Instruments GmbH

Siemensstrasse 9,D-63263 Neu-Isenburg,Germany
 Telephone :+49-6102-297-0 Facsimile :+49-6102-297-320
 Email :info@seiko-instruments.de

Seiko Instruments Inc.

1-8,Nakase,Mihama-ku,Chiba-shi,Chiba 261-8507,Japan
 Facsimile :+81-43-211-8030 E-mail :component@sii.co.jp



We value the "takumi" spirit.

Seiko Instruments Inc.
 Phone:+81-43-211-1207(Direct)

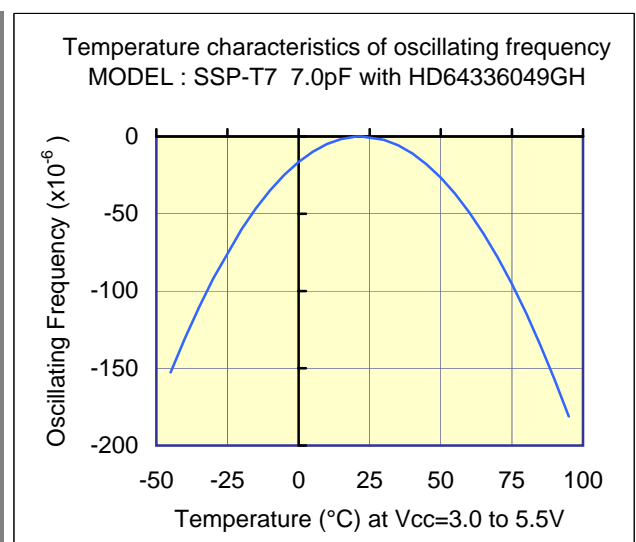
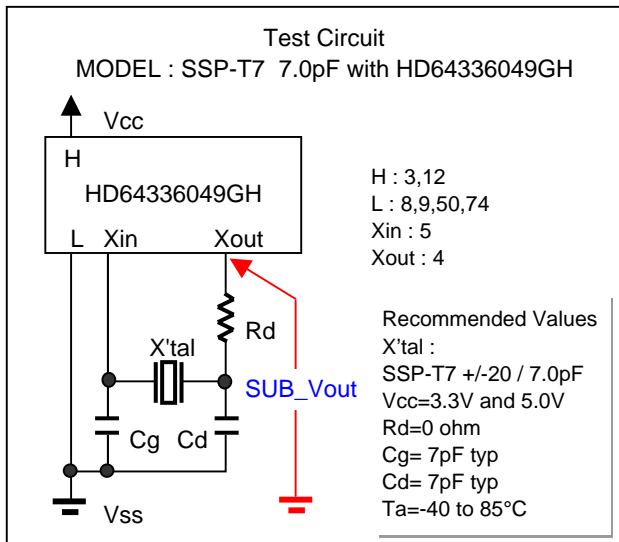
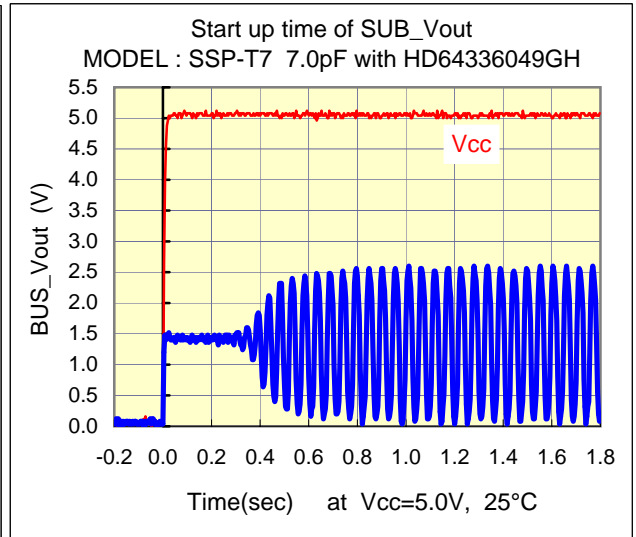
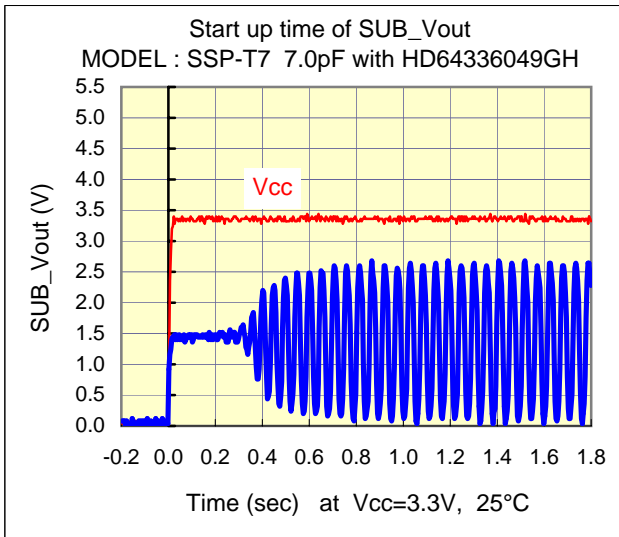
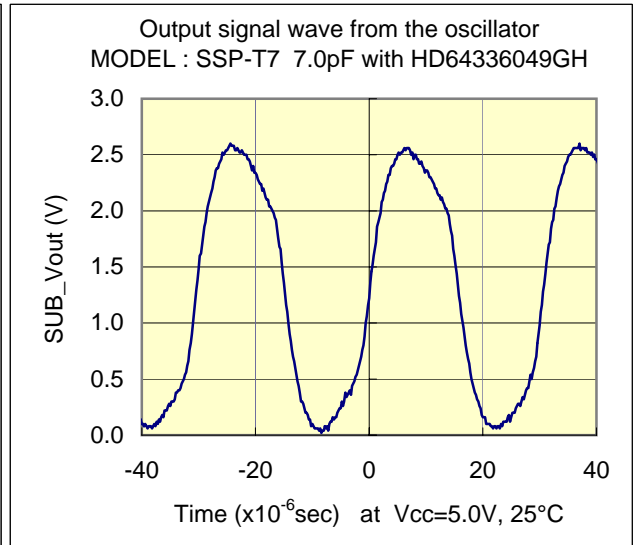
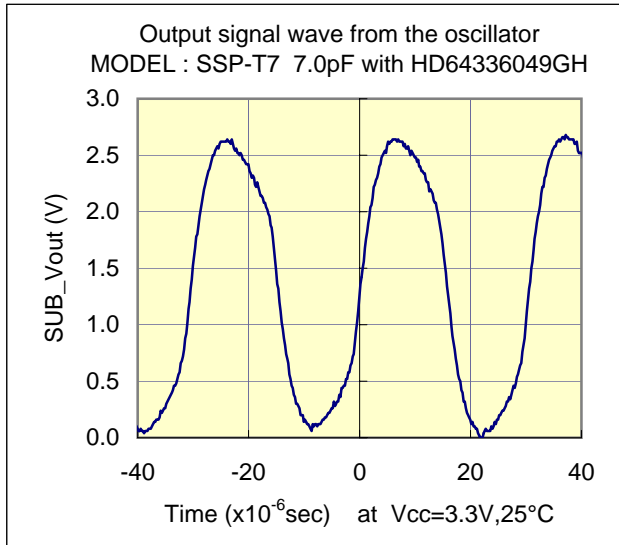
Evaluation of Subsystem Clock Oscillation Circuit

[HD64336049GH] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V (in use of regulator), 3.3V (non use of regulator)



Test Data



Evaluation of Subsystem Clock Oscillation Circuit

[HD64336049GH-80A] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V (in use of regulator), 3.3V (non use of regulator)



Referencial components layout (see Figure 1)

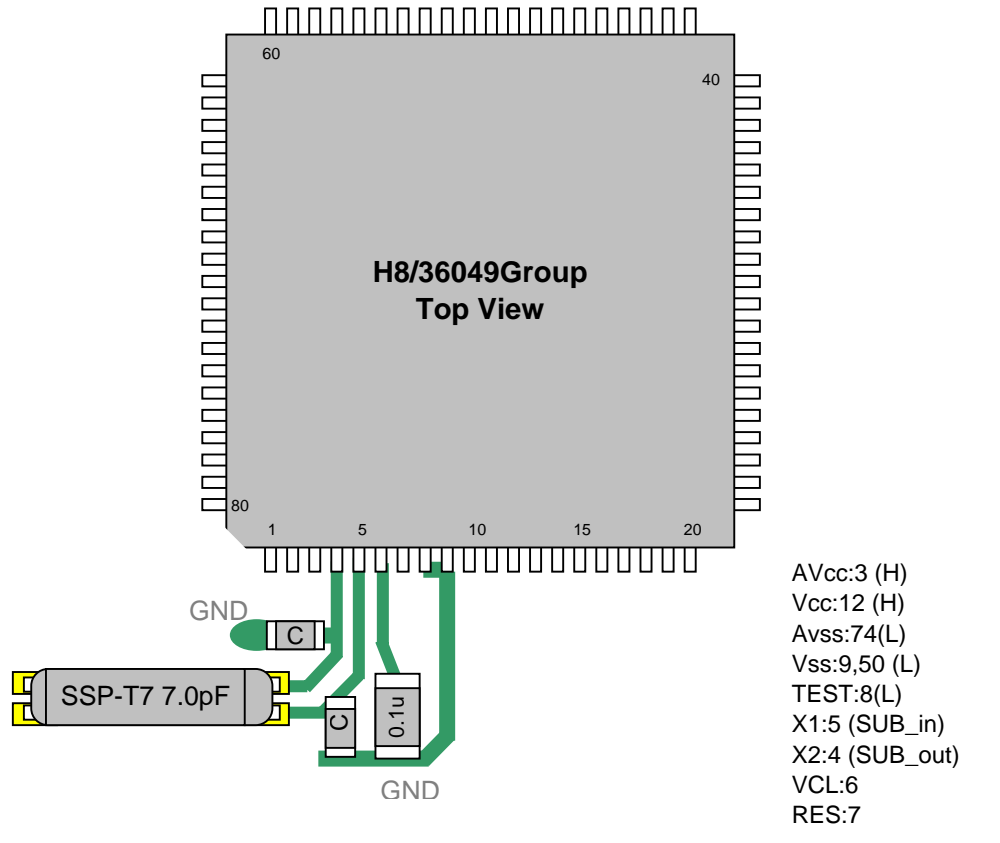


Figure 1 Referencial components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

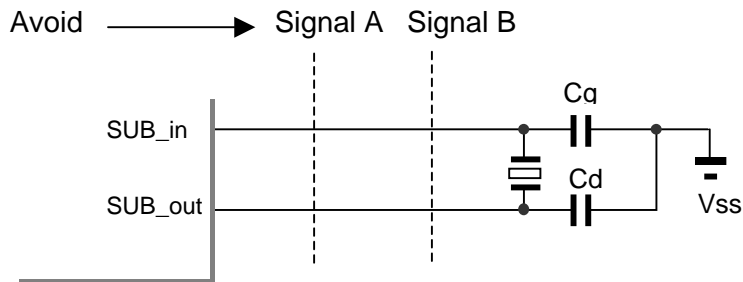


Figure 2 Example of Incorrect Board Design

Evaluation of Subsystem Clock Oscillation Circuit

[HD64336049GH-80A] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V (in use of regulator), 3.3V (non use of regulator)



[Evaluation Sample : SSP-T7 7.0pF at 25°C]

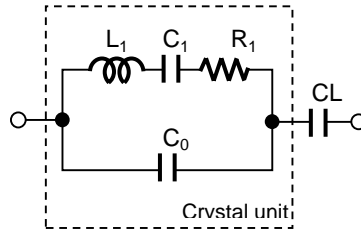
SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
SSP-T7 7.0pF	1	7.0	32768.40	32764.24	37.8	0.83	1.987	64.7
	2	7.0	32767.88	32763.63	39.2	0.85	2.037	60.9
	3	7.0	32767.83	32763.68	40.3	0.83	1.983	60.8

[IC Test Data : IC samples Rd=0 ohm,Cg=7pF,Cd=7pF at 25°C]

Vcc(V)	IC typ	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart(V)	Ts(sec)
5.0	Typ	32768.32	-2.4	0.08	1047	0.99	0.67
	N_low/P_low	32768.37	-0.9	0.06	1047	1.20	0.73
	N_low/P_high	32768.33	-2.1	0.07	1047	1.40	0.70
	N_high/P_low	32768.31	-2.7	0.09	1047	1.53	0.72
	N_high/P_high	32768.28	-3.7	0.09	1047	1.68	0.67
3.3	Typ	32768.30	-3.1	0.08	1047	0.99	0.73
	N_low/P_low	32768.34	-1.8	0.06	1047	1.20	0.69
	N_low/P_high	32768.28	-3.7	0.07	1047	1.40	0.70
	N_high/P_low	32768.30	-3.1	0.09	1047	1.53	0.67
	N_high/P_high	32768.25	-4.6	0.09	1047	1.68	0.61

Remak (see figure 3)

$$F_o = f_r \times \left\{ \frac{C_1}{2 \times (C_o + C_L)} + 1 \right\} \text{ (Hz)}$$



- Fo : Load resonance frequency
- fr : Resonance frequency
- R1 : Motional resistance
- C1 : Motional capacitance
- Co : Shunt capacitance
- CL : Load Capacitance

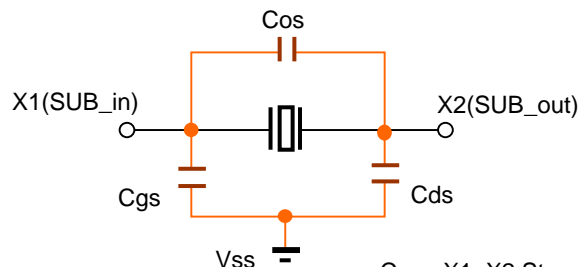
Figure 3 Equivalent circuit of crystal unit, and CL

Remak (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

$$CL = C_g \times C_d / (C_g + C_d) + C_s \text{ (pF)}$$

Where Cs Stands for stray capacity of the circuit.



- Cos : X1_X2 Stray capacitance
- Cgs : X1_Vss Stray capacitance
- Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.