

# Evaluation of Subsystem Clock Oscillation Circuit

[HD64338004H-64A] QFP(14x14) 0.8mm pitch

Measurement conditions : 3.3V , 2.4V

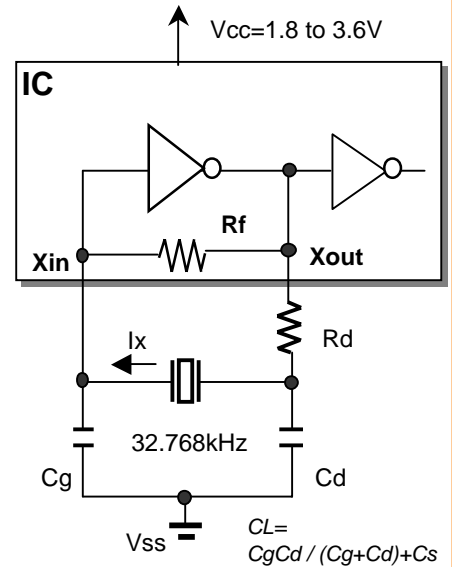
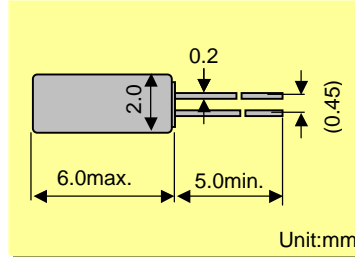


Model :VT-200  
 Frequency :Fo=32.768kHz  
 Frequency tolerance :dF/Fo= +/-20x10<sup>6</sup>  
 Load capacitance :CL=12.5pF  
 Equivalent series resistance :R1=50kohm max  
 Max. Drive level :DL=x10<sup>-6</sup>W max  
 Recommended drive level :DL=0.1x10<sup>-6</sup>W typ

## FEATURES

- 1.Compact tubular package
- 2.Photolithographic process
- 3.Excellent shock resistance and environmental characteristics.
- 4.Real time clocks, Timers, Portable applications

## DIMENSIONS(VT-200)



Remark) Ix : current through crystal

MODEL:VT-200 12.5pF with HD64338004H at 25°C

Key specifications	Vcc=2.4V	Vcc=3.3V	Remarks
Current control resistance : Rd ( k ohm )	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg ( pF )	18	18	Optimal capacity in response to CL
Capacitance at drain : Cd ( pF )	18	18	( CL = Cd // Cg + stray capacitance )

Circuit characteristics ( at 25°C )	Vcc=2.4V	Vcc=3.3V	Remarks
Matching Accuracy : df / f ( x10 <sup>-6</sup> )	-4.9	-1.2	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V ( x10 <sup>-6</sup> )	1.2	1.2	Vdd +/-10% ( Standard operating voltage range )
Drive Level : DL ( x10 <sup>-6</sup> W )	0.28	0.40	DL=Ix <sup>2</sup> Re < 1x10 <sup>-6</sup> W, Re=R1( 1 + Co / CL ) <sup>2</sup>
Negative resistance :   - RL   ( kohm )	654	1234	5 times larger than R <sub>1MAX</sub>
Oscillation allowance : M ( times )	13.1	24.7	Judgemental standard of oscillation stability
Oscillation start up time : Ts ( sec )	0.72	0.57	Time to reach 90% of output level

Temperature characteristics of circuit	Vcc=2.4V	Vcc=3.3V	Remarks
at -40°C Variation : df / T ( x10 <sup>-6</sup> )	-140	-140	Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> )
at +85°C Variation : df / T ( x10 <sup>-6</sup> )	-132	-132	Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> )

The mention value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

### Seiko Instruments USA Inc.

2990,West Lomita Blvd., Torrance, CA 90505, U.S.A  
 Telephone :+1 310-517-7771 Facsimile :+1 310-517-7792  
 Email :crystals@siu-la.com

### Seiko Instruments GmbH

Siemensstrasse 9,D-63263 Neu-Isenburg,Germany  
 Telephone :+49-6102-297-0 Facsimile :+49-6102-297-320  
 Email :info@seiko-instruments.de

### Seiko Instruments Inc.

1-8,Nakase,Mihama-ku,Chiba-shi,Chiba 261-8507,Japan  
 Facsimile :+81-43-211-8030 E-mail :component@sii.co.jp



We value the "takumi" spirit.

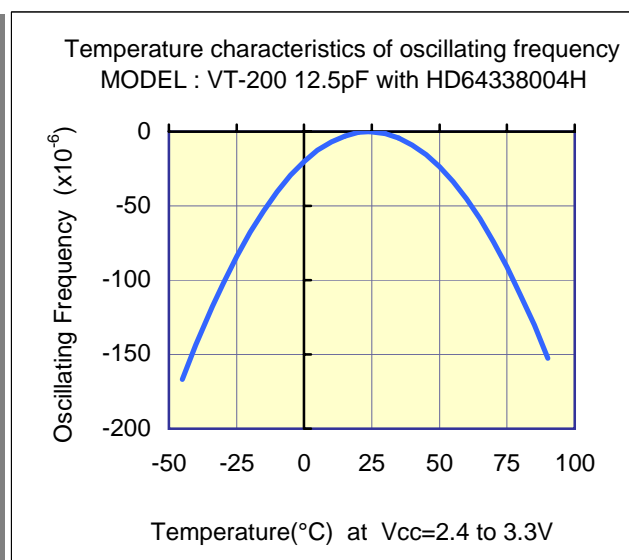
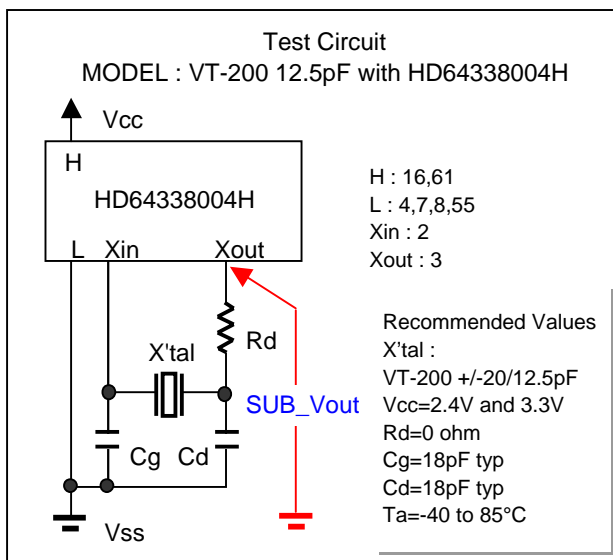
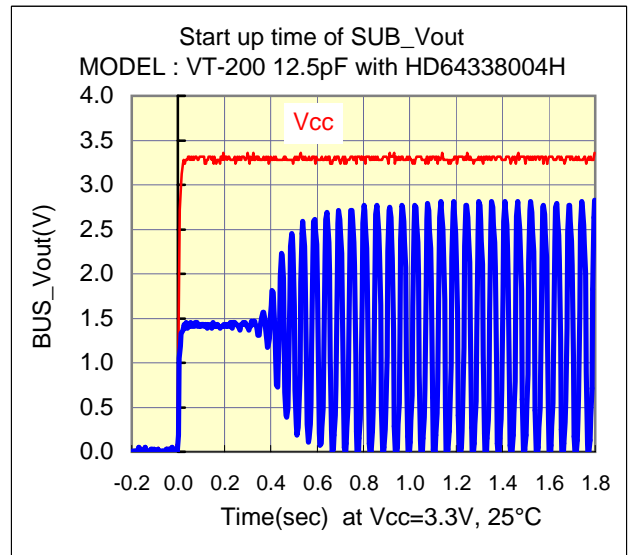
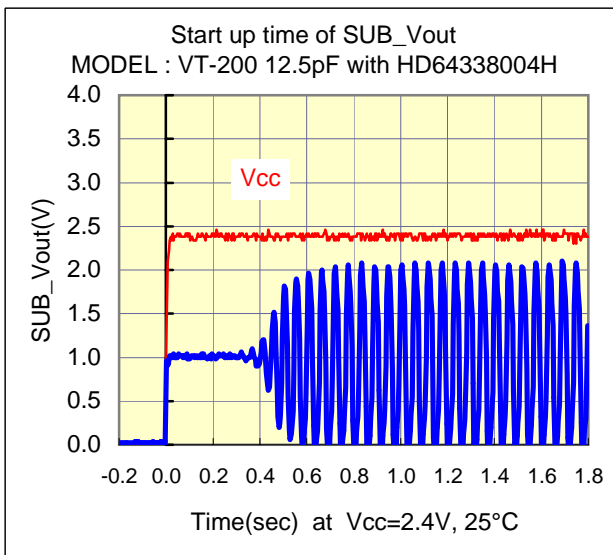
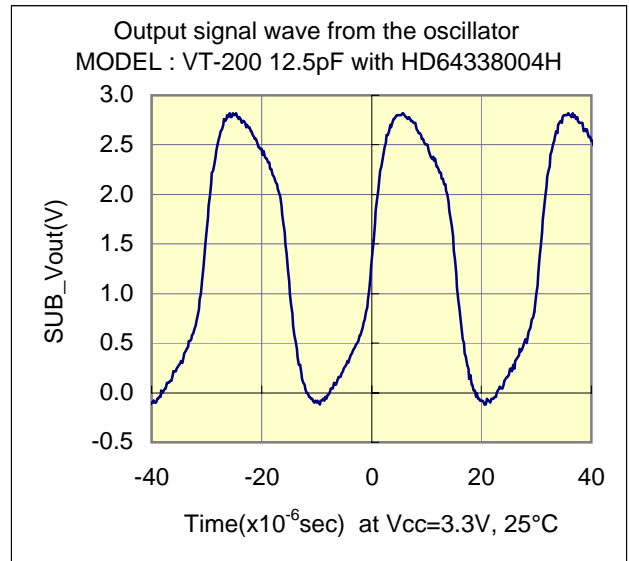
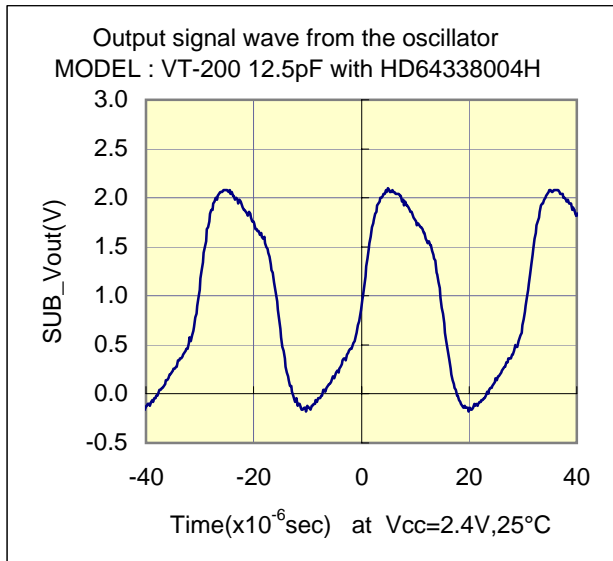
Seiko Instruments Inc.  
 Phone:+81-43-211-1207(Direct)

# Evaluation of Subsystem Clock Oscillation Circuit

[HD64338004H-64A] QFP(14x14) 0.8mm pitch  
 Measurement conditions : 3.3V , 2.4V



## Test Data



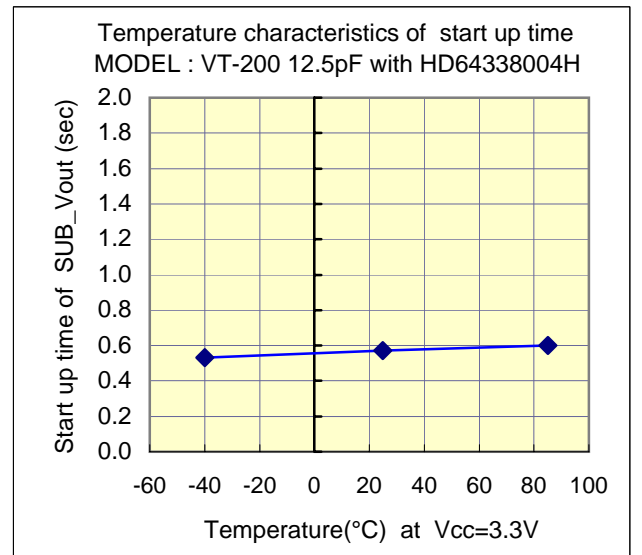
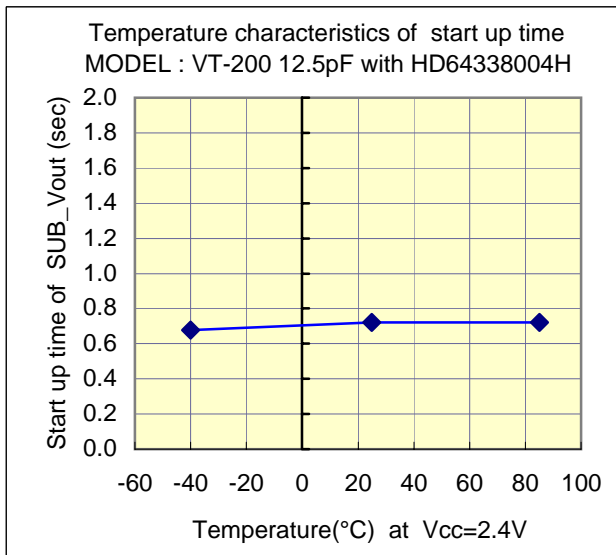
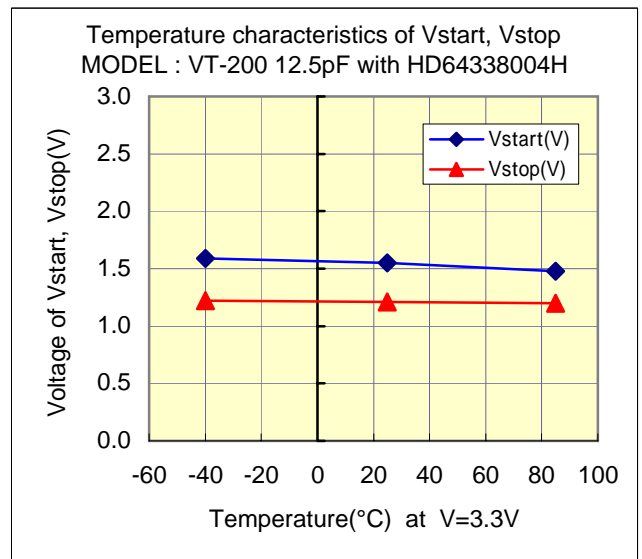
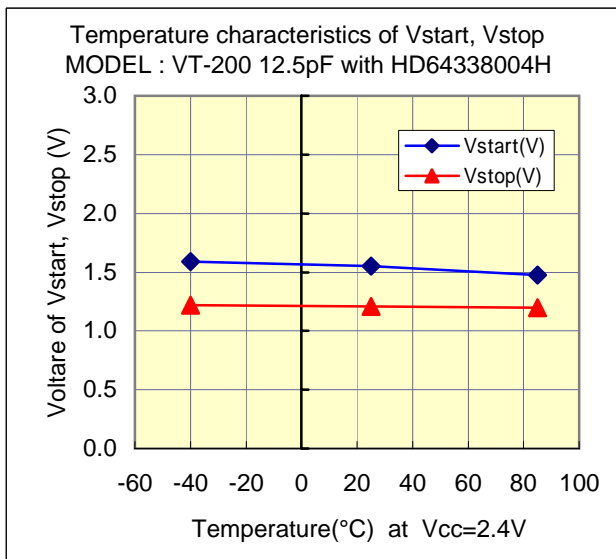
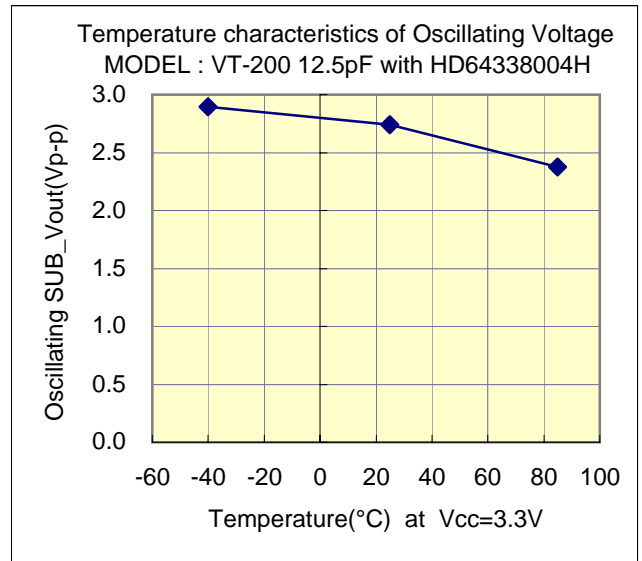
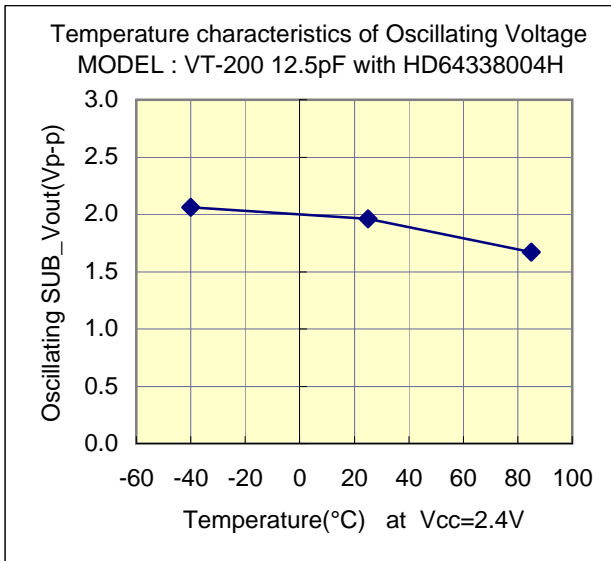
# Evaluation of Subsystem Clock Oscillation Circuit

[HD64338004H-64A] QFP(14x14) 0.8mm pitch

Measurement conditions : 3.3V , 2.4V



## Test Data : Temperature characteristics



# Evaluation of Subsystem Clock Oscillation Circuit

[HD64338004H-64A] QFP(14x14) 0.8mm pitch

Measurement conditions : 3.3V , 2.4V



## Referencial components layout(see Figure 1)

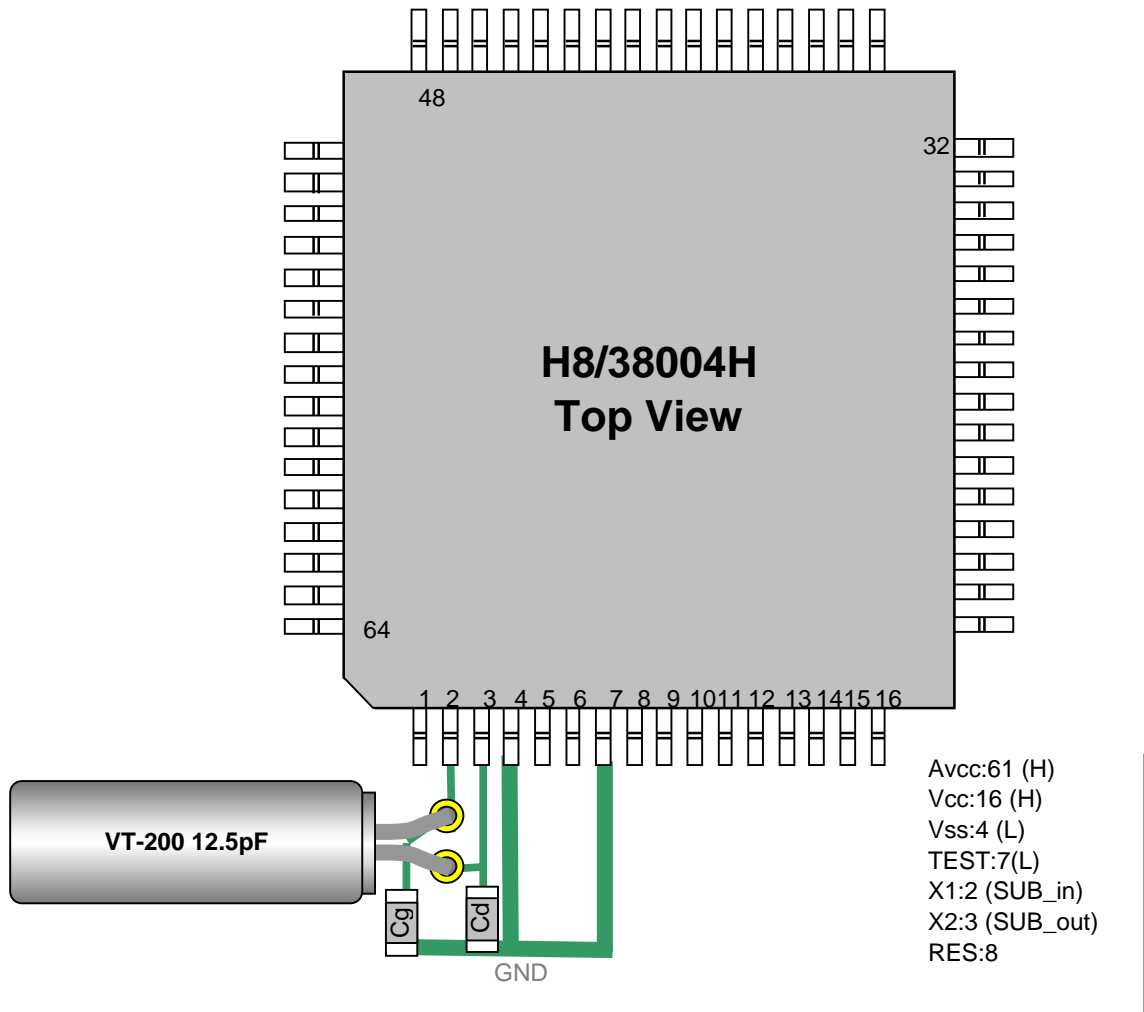


Figure 1 Referencial components layout

## Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB\_in and SUB\_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

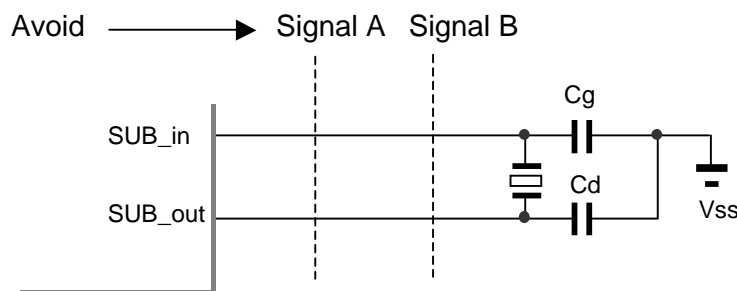


Figure 2 Example of Incorrect Board Design

# Evaluation of Subsystem Clock Oscillation Circuit

[HD64338004H-64A] QFP(14x14) 0.8mm pitch

Measurement conditions : 3.3V , 2.4V



## [Evaluation Sample : VT-200 12.5pF at 25°C]

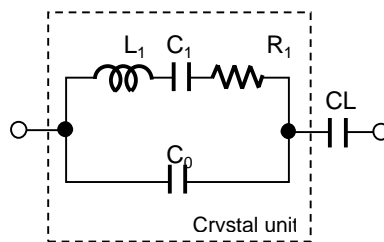
SAMPLE	No.	CL(pF)	Fo( Hz )	fr( Hz )	R1( kohm )	Co( pF )	C1( fF )	Q( k )
VT-200 12.5pF	1	12.5	32768.11	32765.28	27.4	0.91	2.319	76.5
	2	12.5	32768.09	32765.24	26.9	0.89	2.333	77.4
	3	12.5	32768.34	32765.45	29.9	0.93	2.368	68.6

## [IC Test Data : IC samples Rd=0 ohm,Cg=18pF,Cd=18pF at 25°C]

Vcc( V )	IC samples	Fosc( Hz )	df / f( x10 <sup>-6</sup> )	DL(x10 <sup>-6</sup> W)	-RL  ( kohm )	Vstart( V )	Ts(sec)
3.3	W#24-010	32768.30	-1.20	0.40	1234	1.55	0.57
	W#05-006	32768.29	-1.50	0.40	1134	1.50	0.57
	W#09-005	32768.32	-0.59	0.40	1134	1.49	0.59
	W#14-004	32768.32	-0.59	0.40	1134	1.51	0.58
2.4	W#24-010	32768.18	-4.86	0.28	654	1.55	0.72
	W#05-006	32768.20	-4.25	0.28	654	1.50	0.73
	W#09-005	32768.21	-3.94	0.28	654	1.49	0.71
	W#14-004	32768.20	-4.25	0.28	654	1.51	0.76

Remak ( see figure 3 )

$$F_o = f_r \times \left\{ \frac{C_1}{2 \times (C_o + C_L)} + 1 \right\} \text{ ( Hz )}$$



- Fo : Load resonance frequency
- fr : Resonance frequency
- R1 : Motional resistance
- C1 : Motional capacitance
- Co : Shunt capacitance
- CL : Load Capacitance

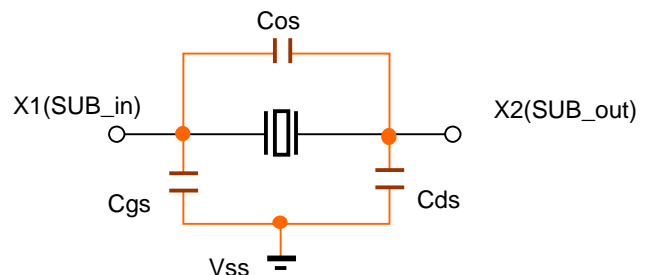
Figure 3 Equivalent circuit of crystal unit, and CL

Remak ( see figure 4 )

Approximate formula of the load capacitance of the circuit CL.

$$CL = C_g \times C_d / (C_g + C_d) + C_s \text{ ( pF )}$$

Where Cs Stands for stray capacity of the circuit.



- Cos : X1\_X2 Stray capacitance
- Cgs : X1\_Vss Stray capacitance
- Cds : X2\_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.