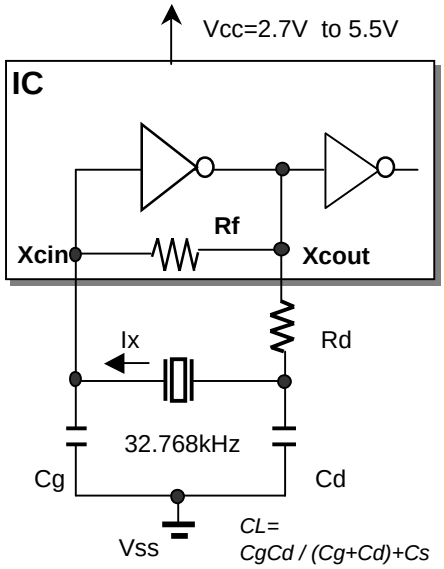
Evaluation of Subsystem Clock Oscillation Circuit

[M30626FJPFP-100P] QFP(14x20) 0.65mm pitch

Measurement conditions : 5.0V

Model	:VT-200
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10^{6}
Load capacitance	:CL=12.5pF
Equivalent series resistance	:R1=50kohm max
Max. Drive level	:DL=1x10^{-6}W max
Recommended drive level	:DL=0.1x10^{-6}W typ

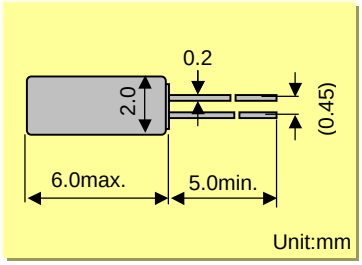


Remark) Ix : current through crystal

FEATURES

1.Compact tubular package
2.Photolithographic process
3.Excellent shock resistance and environmental characteristics.
4.Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)



*When the product with its load capacitance = 12.5pF is used, please make sure the drive mode is set up high.
*When the product is used with the low drive mode setup, our product with its load capacitance = 6.0pF is recommended.

MODEL:VT-200 12.5pF with M30626FJPFP at Vcc=5.0V,25°C

Key specifications	Low	High	Remarks
Current control resistance : Rd (k ohm)	220	220	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	15	18	Optimal capacity in response to CL
Capacitance at drain : Cd (pF)	15	18	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Low	High	Remarks
Matching Accuracy : df / f (x10^{-6})	-1.2	0.0	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V (x10^{-6})	0.6	0.4	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL (x10^{-6}W)	0.12	0.22	DL=Ix^{2} Re < 1x10^{-6}W,Re=R1(1 + Co / CL)^{2}
Negative resistance : | - RL | (kohm)	144	944	5 times larger than R_{1MAX} : ($5*50k=250kohm_{min}$)
Oscillation allowance : M (times)	2.9	18.9	Judgemental standard of oscillation stability
Oscillation start up time : Ts (sec)	-	0.28	Time to reach 90% of output level

Temperature characteristics of circuit		Low	High	Remarks
at -40°C	Variation : df / T (x10^{-6})	-140	-139	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^{2})
at +85°C	Variation : df / T (x10^{-6})	-134	-135	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^{2})

The mention value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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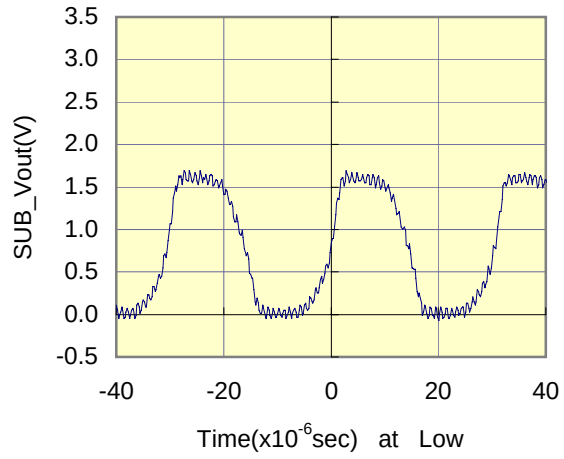
Evaluation of Subsystem Clock Oscillation Circuit

[M30626FJPFP-100P] QFP(14x20) 0.65mm pitch

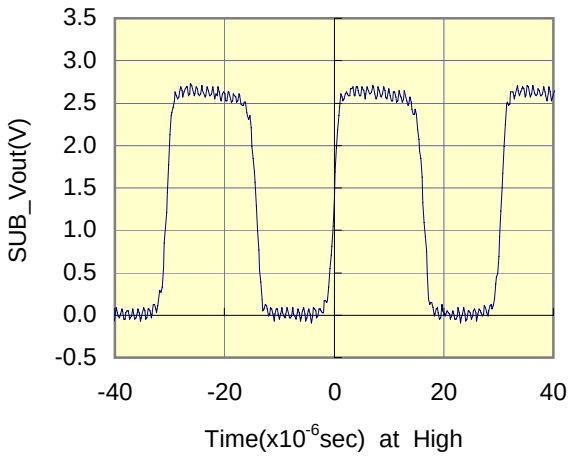
Measurement conditions : 5.0V

Test Data at Vcc=3.3V to 5.0V,25°C

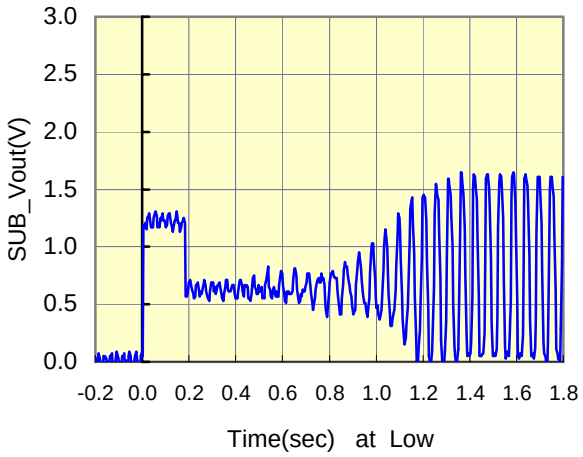
Output signal wave from the oscillator
MODEL : VT-200 12.5pF with M30626FJPFP



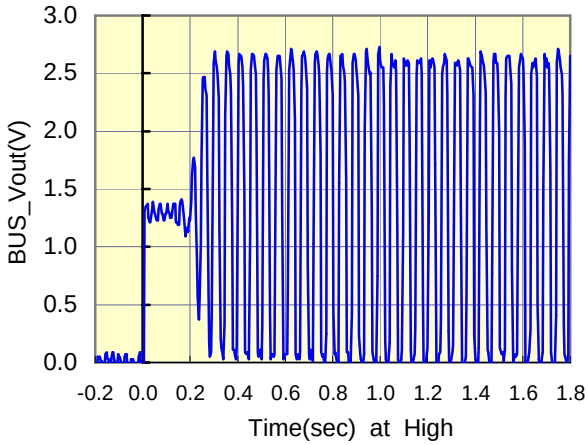
Output signal wave from the oscillator
MODEL : VT-200 12.5pF with M30626FJPFP



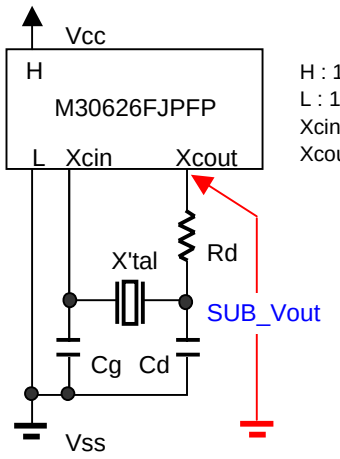
Start up time of SUB_Vout
MODEL : VT-200 12.5pF with M30626FJPFP



Start up time of SUB_Vout
MODEL : VT-200 12.5pF with M30626FJPFP



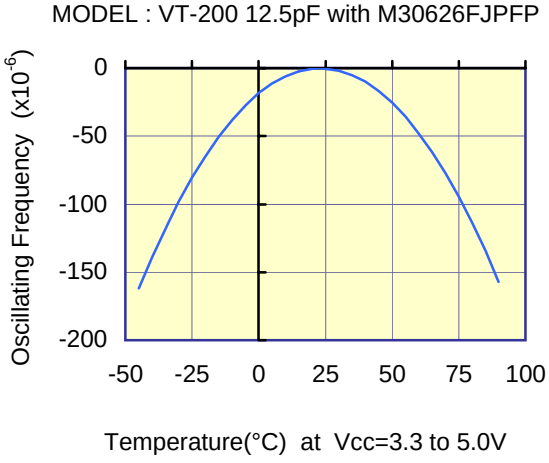
Test Circuit
MODEL : VT-200 12.5pF with M30626FJPFP



H : 16,62,99
L : 14,64,96
Xcin : 10
Xcout : 11

Recommended Values
X'tal :
VT-200 +/-20/12.5pF
Vcc=3.3V to 5.0V
Rd=220k ohm
Cg=15 to 18pF typ
Cd=15 to 18pF typ
Ta=-40 to 85°C

Temperature characteristics of oscillating frequency
MODEL : VT-200 12.5pF with M30626FJPFP



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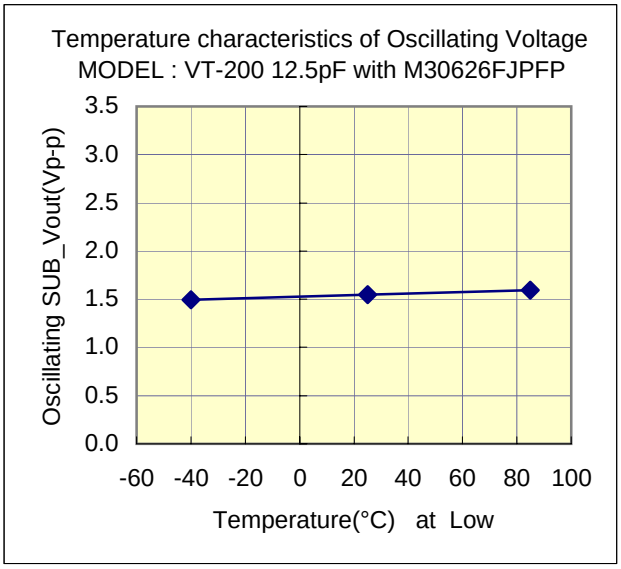
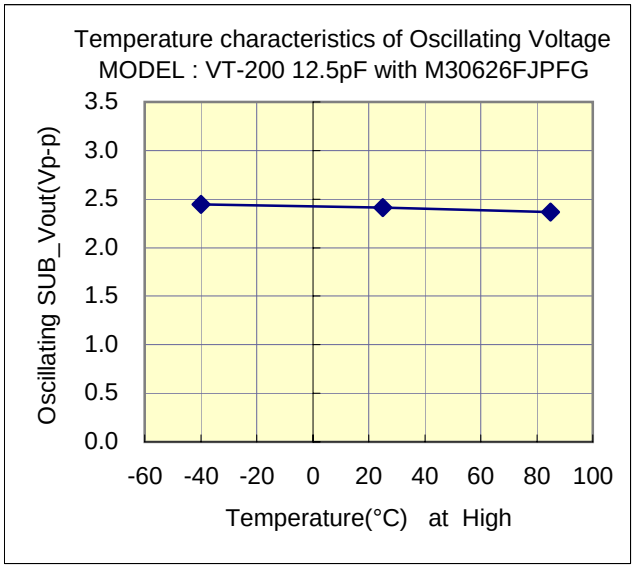
Evaluation of Subsystem Clock Oscillation Circuit

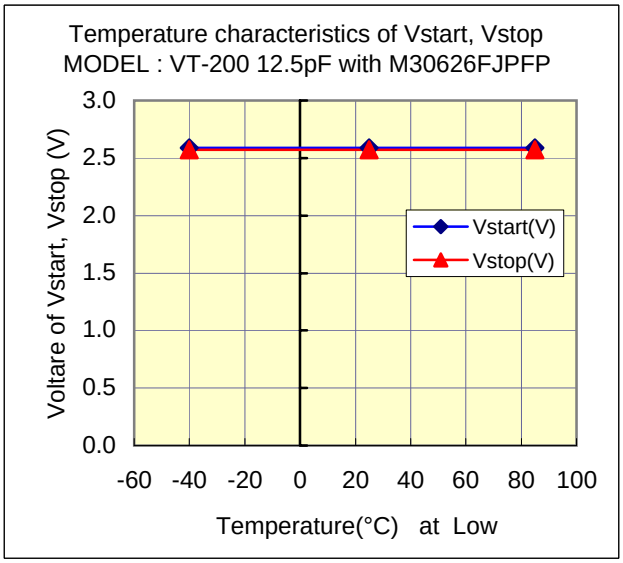
[M30626FJPFP-100P] QFP(14x20) 0.65mm pitch

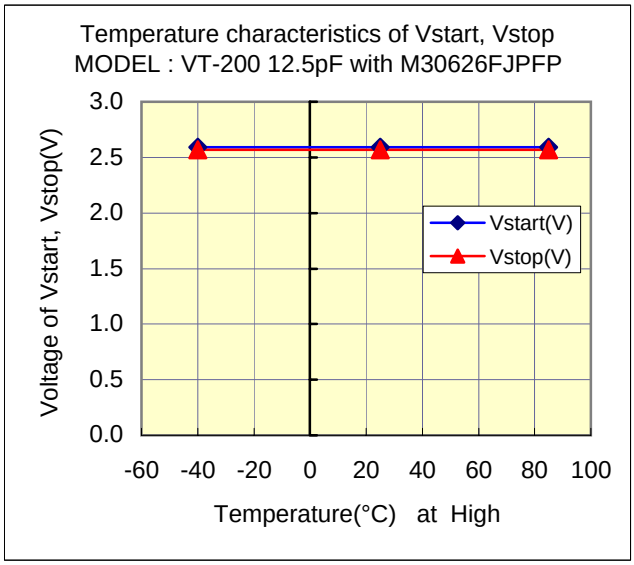
Measurement conditions : 5.0V

Test Data : Temperature characteristics at Vcc=3.3V to 5.0V









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Evaluation of Subsystem Clock Oscillation Circuit

[M30626FJPFP-100P] QFP(14x20) 0.65mm pitch
Measurement conditions : 5.0V

Referenicial components layout(see Figure 1)

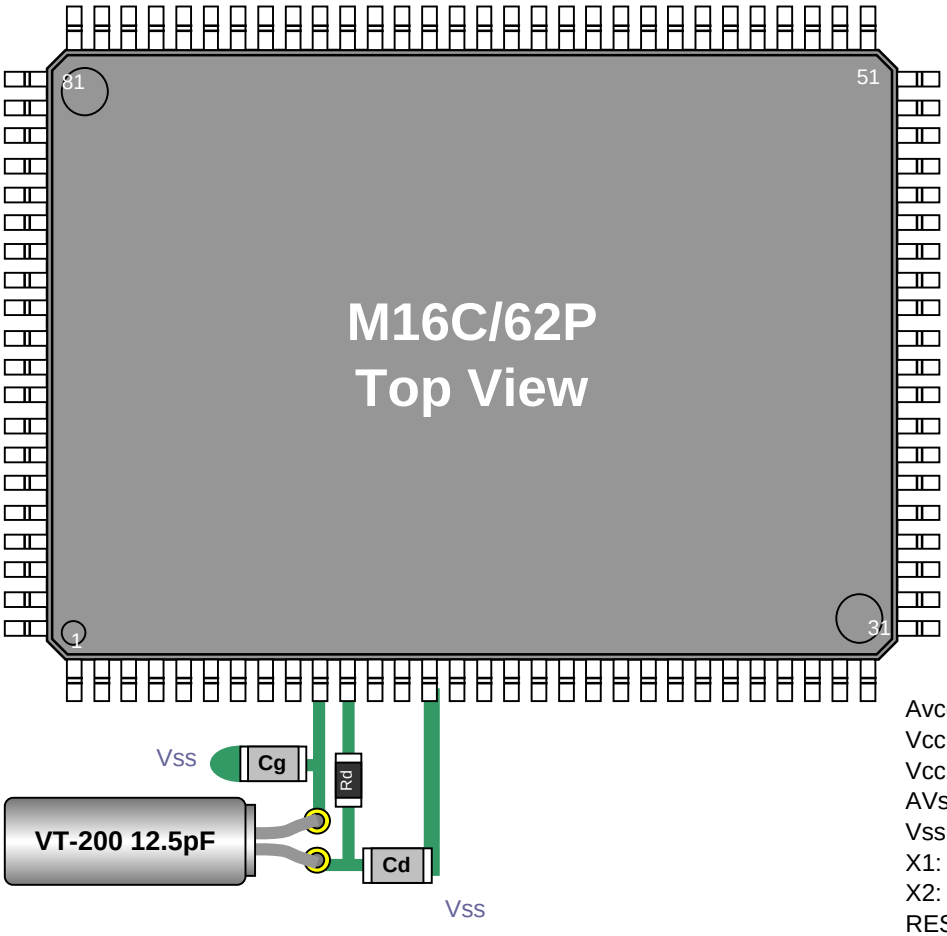

Figure 1 Referenicial components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.
Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

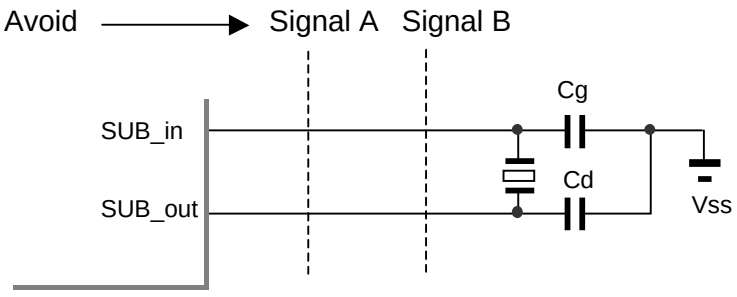

Figure 2 Example of Incorrect Board Design

Remak When using the subsystem clock, insert resistors Rd in series on the SUB_out side.

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Measurement conditions : 5.0V

[Evaluation Sample : VT-200 12.5pF at 25°C]

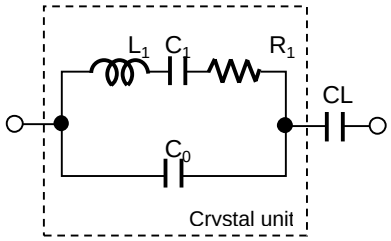
SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
VT-200 12.5pF	1	12.5	32768.11	32765.28	27.4	0.91	2.319	76.5
	2	12.5	32768.09	32765.24	26.9	0.89	2.333	77.4
	3	12.5	32768.34	32765.45	29.9	0.93	2.368	68.6

[IC Test Data : IC samples Rd=220k ohm,Cg=15 to 18pF,Cd=15 to 18pF at 25°C]

Mode	IC samples	Fosc(Hz)	df / f(x10^{-6})	DL(x10^{-6}W)	| -RL |(kohm)	Vstart(V)	Ts(sec)
High	TYP	32768.34	-0.04	0.22	944	2.59	0.28
	HHD	32768.40	1.86	0.11	1034	2.59	0.47
	LLD	32768.38	1.25	0.12	784	2.59	0.52
Low_NG	TYP	32768.30	-1.20	0.12	**144**	2.59	-
	HHD	32768.40	1.86	0.13	**125**	2.59	-
	LLD	32768.28	-1.68	0.11	**194**	2.59	-

Remak (see figure 3)

Fo = fr ×{ C1/ (2×(Co + CL) + 1 } (Hz)



Fo : Load resonance frequency
fr : Resonance frequency
R1 : Motional resistance
C1 : Motional capacitance
Co : Shunt capacitance
CL : Load Capacitance

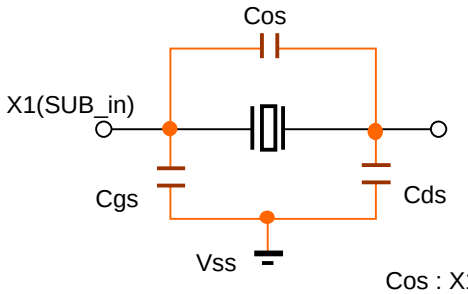
Figure 3 Equivalent circuit of crystal unit, and CL

Remak (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

CL = Cg×Cd / (Cg + Cd) + Cs (pF)

Where Cs Stands for stray capacity of the circuit.



Cos : X1_X2 Stray capacitance
Cgs : X1_Vss Stray capacitance
Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

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