

Evaluation of Subsystem Clock Oscillation Circuit

[uPD780114GB-8ES] LQFP(10x10) 0.8mm pitch

Measurement conditions : 5.0V , 3.3V

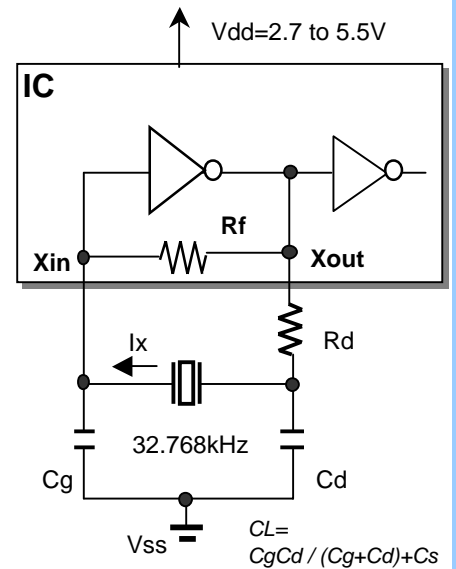
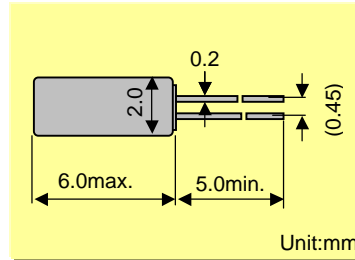


Model	:VT-200
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10 ⁶
Load capacitance	:CL=6.0pF
Equivalent series resistance	:R1=50kohm max
Max. Drive level	:DL=x10 ⁻⁶ W max
Recommended drive level	:DL=0.1x10 ⁻⁶ W typ

FEATURES

- 1.Compact tubular package
- 2.Photolithographic process
- 3.Excellent shock resistance and environmental characteristics.
- 4.Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)



Remark) I_x : current through crystal

MODEL:VT-200 6.0pF with uPD780114GB at 25°C

Key specifications	Vdd=3.3V	Vdd=5.0V	Remarks
Current control resistance : Rd (k ohm)	220	220	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	6	8	Optimal capacity in response to CL
Capacitance at drain : Cd (pF)	5	7	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vdd=3.3V	Vdd=5.0V	Remarks
Matching Accuracy : df / f ($\times 10^{-6}$)	-1.2	-1.8	Frequency offset volume at specified Vdd
Voltage Fluctuation : $\pm df / V$ ($\times 10^{-6}$)	5.4	6.1	Vdd $\pm 10\%$ (Standard operating voltage range)
Drive Level : DL ($\times 10^{-6}$ W)	0.03	0.04	$DL = I_x^2 R_e < 1 \times 10^{-6}$ W, $R_e = R_1(1 + C_o / CL)^2$
Negative resistance : $ -RL $ (kohm)	788	948	5 times larger than R_{1MAX}
Oscillation allowance : M (times)	15.8	19.0	Judgemental standard of oscillation stability
Oscillation start up time : Ts (sec)	0.67	0.63	Time to reach 90% of output level

Temperature characteristics of circuit	Vdd=3.3V	Vdd=5.0V	Remarks
at -40°C Variation : df / T ($\times 10^{-6}$)	-131	-131	Typ.Tp=25°C (K = $-3.5 \times 10^{-8} / ^\circ\text{C}^2$)
at +85°C Variation : df / T ($\times 10^{-6}$)	-137	-138	Typ.Tp=25°C (K = $-3.5 \times 10^{-8} / ^\circ\text{C}^2$)

The mention value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

Seiko Instruments USA Inc.

2990,West Lomita Blvd., Torrance, CA 90505, U.S.A
 Telephone :+1 310-517-7771 Facsimile :+1 310-517-7792
 Email :crystals@siu-la.com

Seiko Instruments GmbH

Siemensstrasse 9,D-63263 Neu-Isenburg,Germany
 Telephone :+49-6102-297-0 Facsimile :+49-6102-297-320
 Email :info@seiko-instruments.de

Seiko Instruments Inc.

1-8,Nakase,Mihama-ku,Chiba-shi,Chiba 261-8507,Japan
 Facsimile :+81-43-211-8030 E-mail :component@sii.co.jp



We value the "takumi" spirit.

Seiko Instruments Inc.

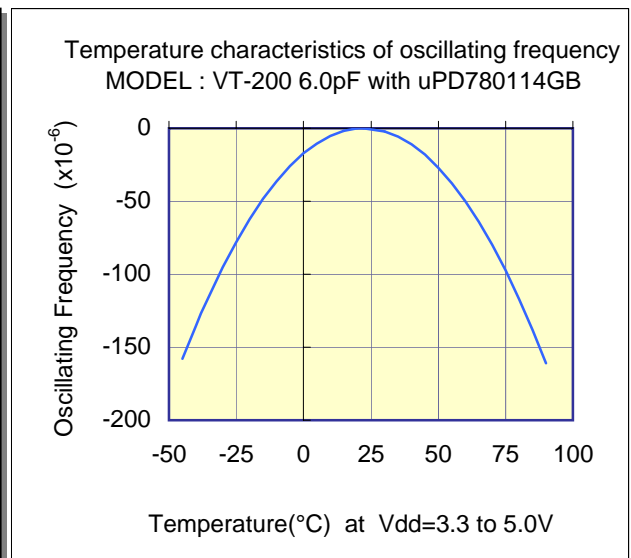
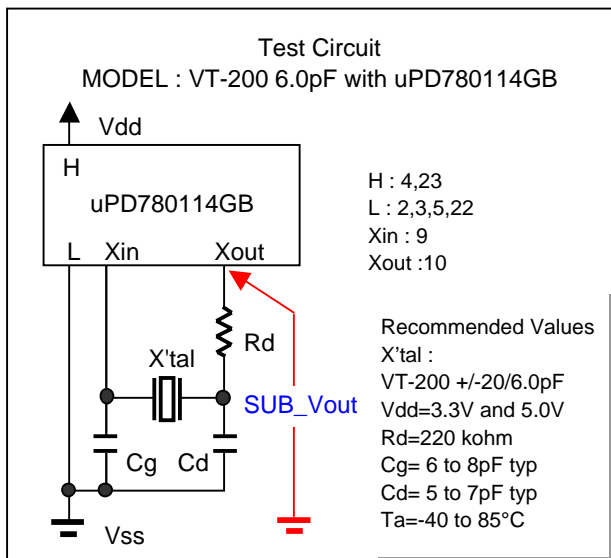
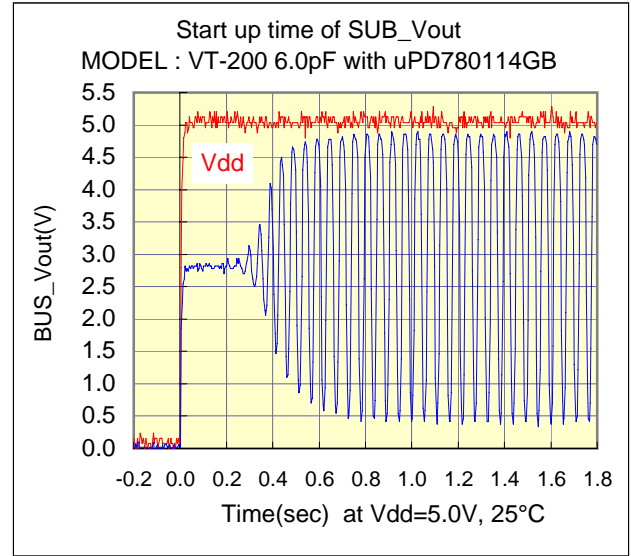
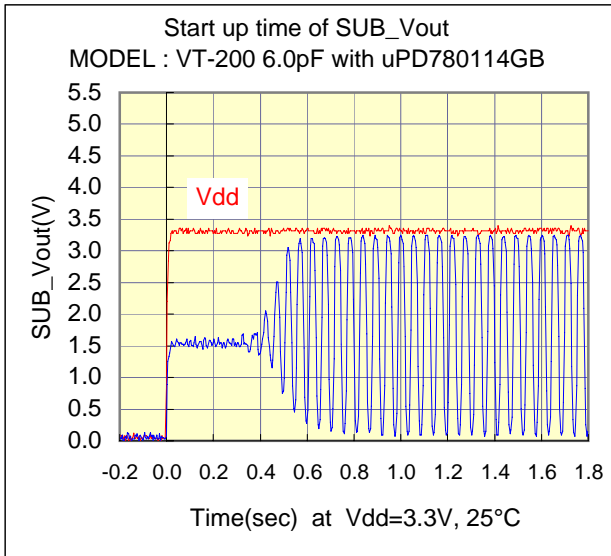
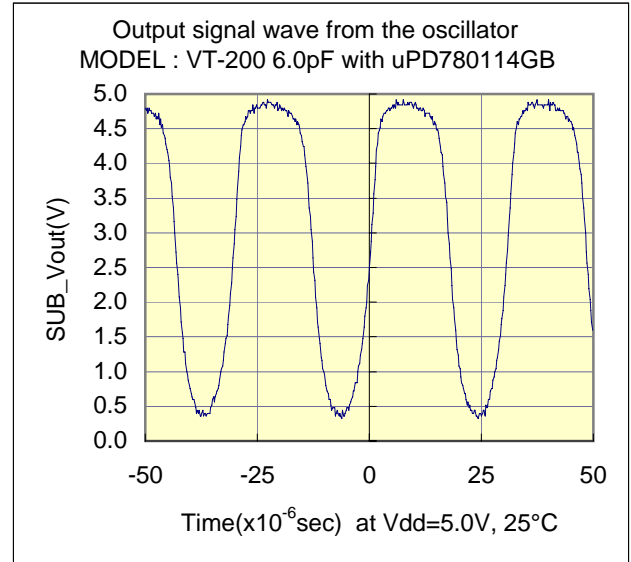
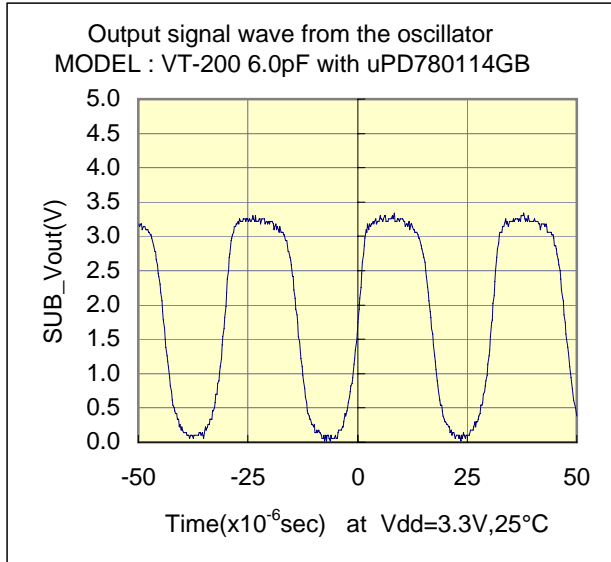
Phone:+81-43-211-1207(Direct)

Evaluation of Subsystem Clock Oscillation Circuit

[uPD780114GB-8ES] LQFP(10x10) 0.8mm pitch
 Measurement conditions : 5.0V , 3.3V



Test Data

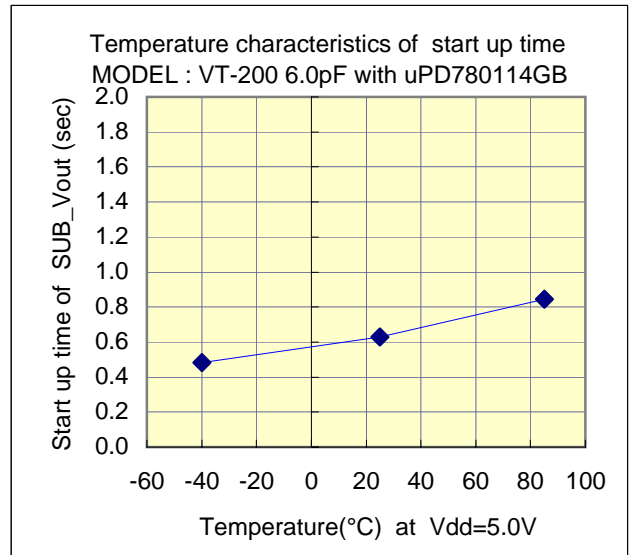
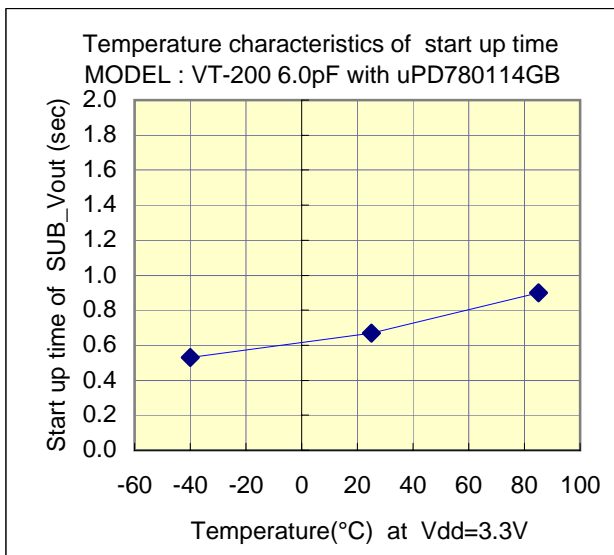
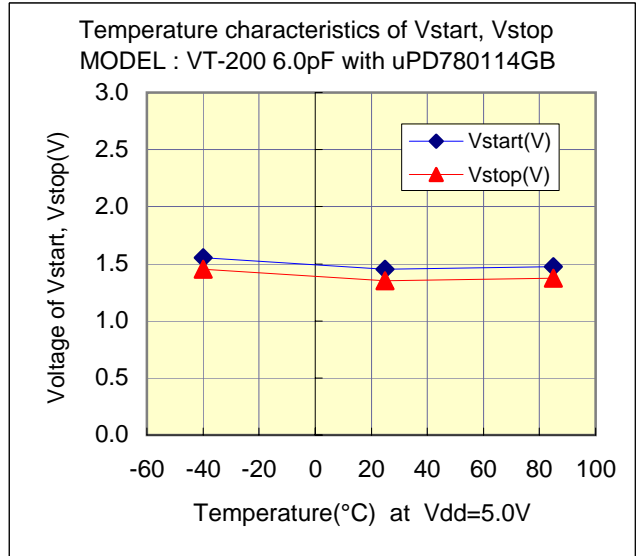
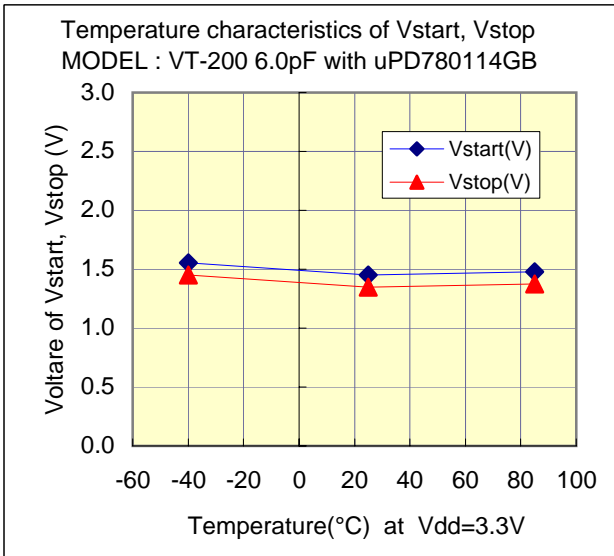
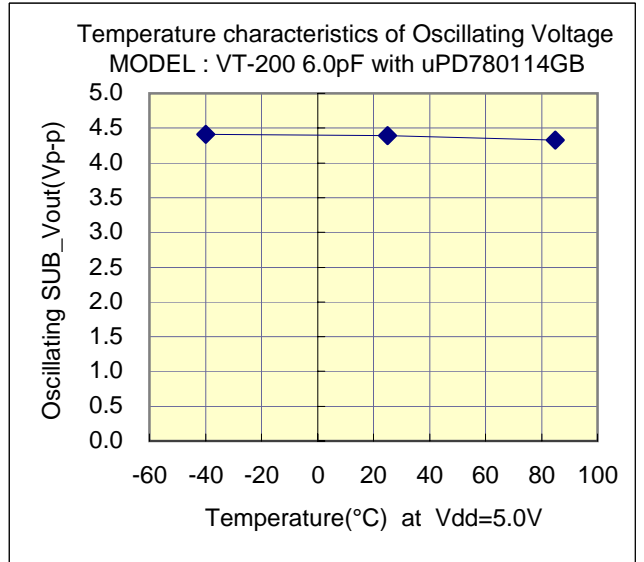
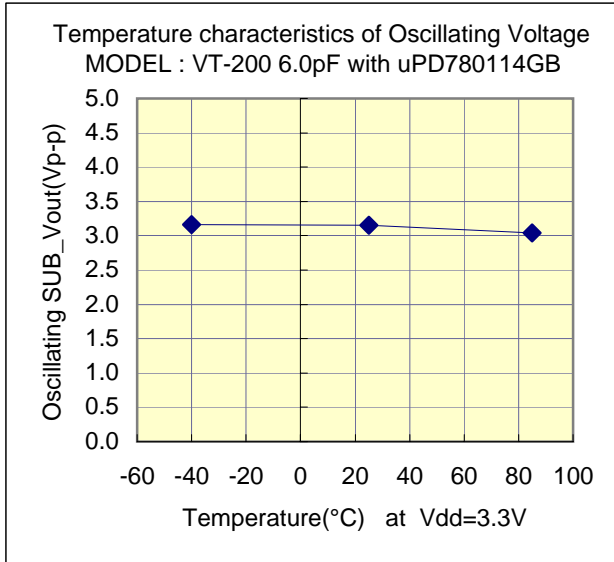


Evaluation of Subsystem Clock Oscillation Circuit

[uPD780114GB-8ES] LQFP(10x10) 0.8mm pitch
 Measurement conditions : 5.0V , 3.3V



Test Data : Temperature characteristics



Evaluation of Subsystem Clock Oscillation Circuit

[μ PD780114GB-8ES] LQFP(10x10) 0.8mm pitch

Measurement conditions : 5.0V , 3.3V

Referencial components layout(see Figure 1)

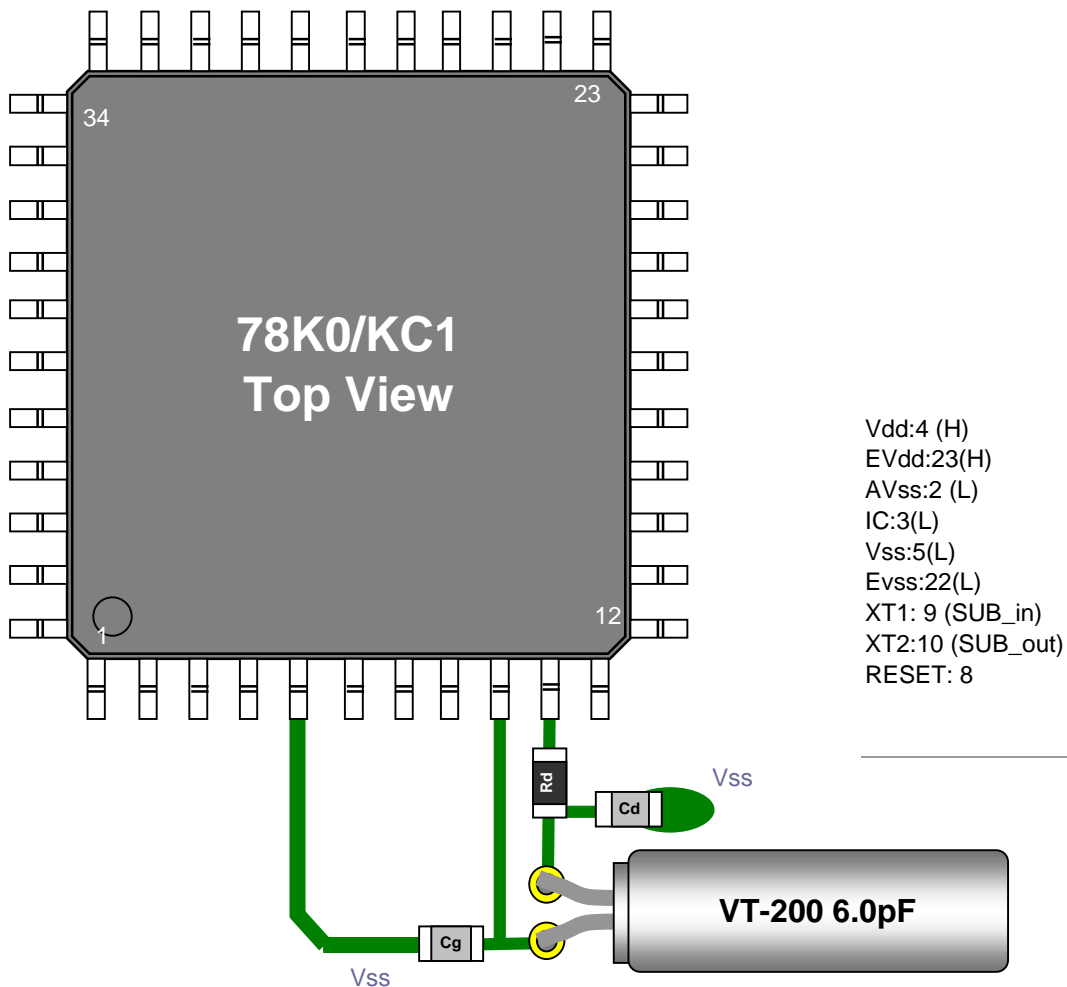


Figure 1 Referencial components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

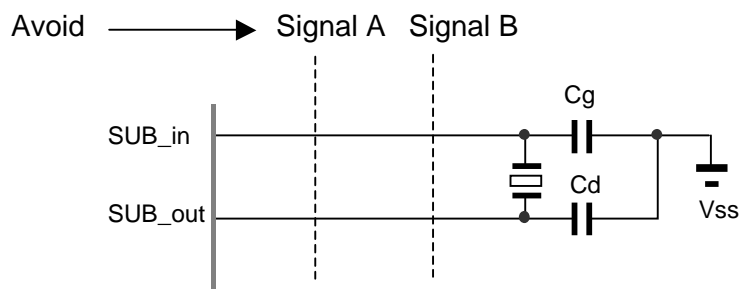


Figure 2 Example of Incorrect Board Design

Remak When using the subsystem clock, insert resistors R_d in series on the SUB_out side.

Evaluation of Subsystem Clock Oscillation Circuit

[uPD780114GB-8ES] LQFP(10x10) 0.8mm pitch

Measurement conditions : 5.0V , 3.3V



[Evaluation Sample : VT-200 6.0pF at 25°C]

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
VT-200 6.0pF	1	6	32768.18	32762.98	28.7	0.91	2.193	77.2
	2	6	32768.18	32763.04	27.8	0.89	2.161	80.9
	3	6	32768.19	32763.00	27.2	0.90	2.187	81.7

[IC Test Data : IC Sampl Rd=220kohm,Cg=8pF,Cd=7pF at 25°C]

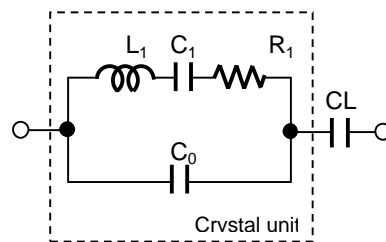
Vdd(V)	IC Sampl	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart(V)	Ts(sec)
5.0	typ-#01	32768.12	-1.83	0.04	948.1	1.45	0.63
	typ-#02	32768.13	-1.53	0.04	948.1	1.44	0.60
	typ-#03	32768.13	-1.59	0.04	948.1	1.45	0.66

[IC Test Data : IC Sampl Rd=220kohm,Cg=6pF,Cd=5pF at 25°C]

Vdd(V)	IC Sampl	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart(V)	Ts(sec)
3.3	typ-#01	32768.14	-1.22	0.03	788.1	1.45	0.67
	typ-#02	32768.14	-1.22	0.03	788.1	1.45	0.66
	typ-#03	32768.14	-1.31	0.03	788.1	1.45	0.72

Remak (see figure 3)

$$F_o = f_r \times \left\{ \frac{C_1}{2 \times (C_o + C_L)} + 1 \right\} \text{ (Hz)}$$



Fo : Load resonance frequency
 fr : Resonance frequency
 R1 : Motional resistance
 C1 : Motional capacitance
 Co : Shunt capacitance
 CL : Load Capacitance

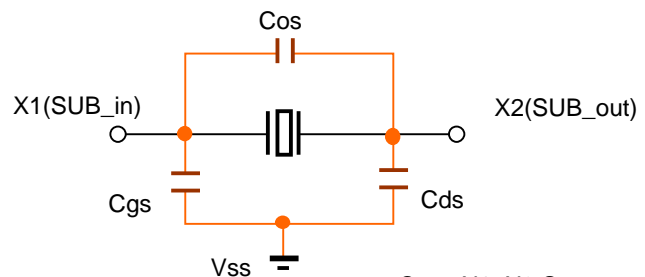
Figure 3 Equivalent circuit of crystal unit, and CL

Remak (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

$$CL = C_g \times C_d / (C_g + C_d) + C_s \text{ (pF)}$$

Where Cs Stands for stray capacity of the circuit.



Cos : X1_X2 Stray capacitance
 Cgs : X1_Vss Stray capacitance
 Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

