

# Evaluation of Subsystem Clock Oscillation Circuit

[uPD780114GB-8ES] LQFP(10x10) 0.8mm pitch

Measurement conditions : 5.0V , 3.3V

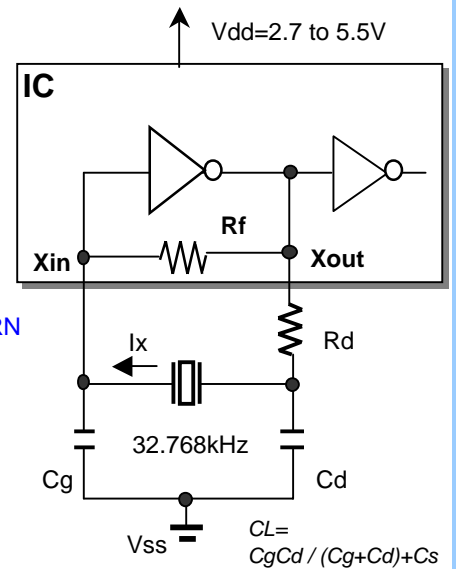
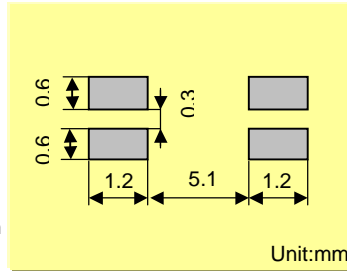


Model	:SSP-T7
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10 <sup>6</sup>
Load capacitance	:CL=7.0pF
Equivalent series resistance	:R1=65kohm max
Max. Drive level	:DL=x10 <sup>-6</sup> W max
Recommended drive level	:DL=0.1x10 <sup>-6</sup> W typ

## FEATURES

- 1.Ultra thin type with 1.4mm Max.
- 2.SMD type suitable for automatic & high density surface mounting.
- 3.Plastic mold package containing highly reliable tubular type quartz crystal.
- 4.Excellent shock and heat resistance.
- 5.Cellular phones,PDA,Radio communication equipment, Portable applications etc.

## RECOMMENDED SOLDERIN PATTERN



Remark) Ix : current through crystal

MODEL:SSP-T7 7.0pF with uPD780114GB at 25°C

Key specifications	Vdd=3.3V	Vdd=5.0V	Remarks
Current control resistance : Rd ( k ohm )	220	220	Control drive level & secure phase margin
Capacitance at gate : Cg ( pF )	7	9	Optimal capacity in response to CL
Capacitance at drain : Cd ( pF )	7	9	( CL = Cd // Cg + stray capacitance )

Circuit characteristics ( at 25°C )	Vdd=3.3V	Vdd=5.0V	Remarks
Matching Accuracy : df / f ( x10 <sup>-6</sup> )	2.4	1.5	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V ( x10 <sup>-6</sup> )	4.0	4.3	Vdd +/-10% ( Standard operating voltage range )
Drive Level : DL ( x10 <sup>-6</sup> W )	0.05	0.08	DL=Ix <sup>2</sup> Re < 1x10 <sup>-6</sup> W, Re=R1( 1 + Co / CL ) <sup>2</sup>
Negative resistance :   - RL   ( kohm )	800	870	5 times larger than R1MAX
Oscillation allowance : M ( times )	12.3	13.4	Judgemental standard of oscillation stability
Oscillation start up time : Ts ( sec )	0.78	0.70	Time to reach 90% of output level

Temperature characteristics of circuit	Vdd=3.3V	Vdd=5.0V	Remarks	
at -40°C	Variation : df / T ( x10 <sup>-6</sup> )	-134	-135	Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> )
at +85°C	Variation : df / T ( x10 <sup>-6</sup> )	-136	-136	Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> )

The mention value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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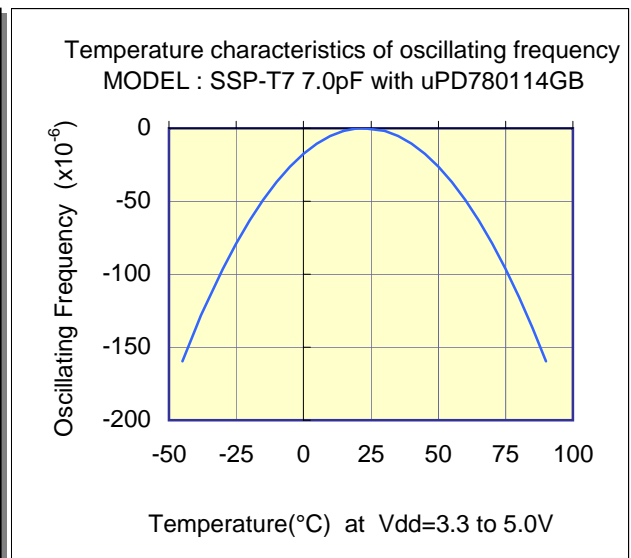
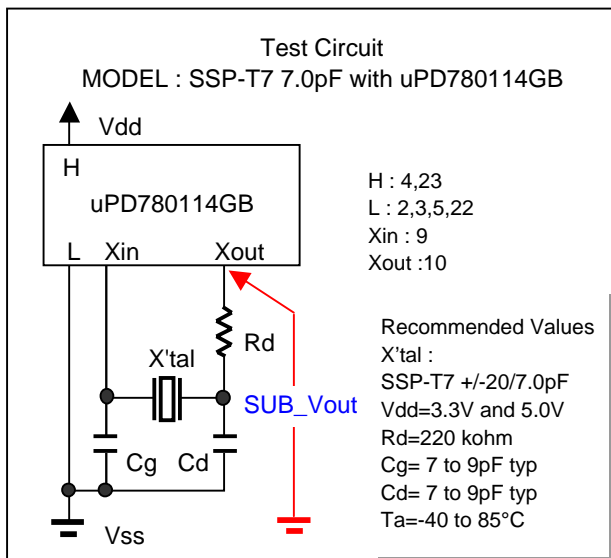
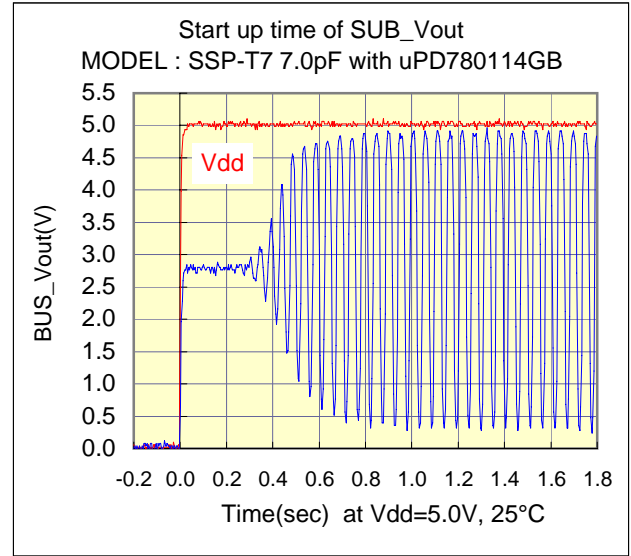
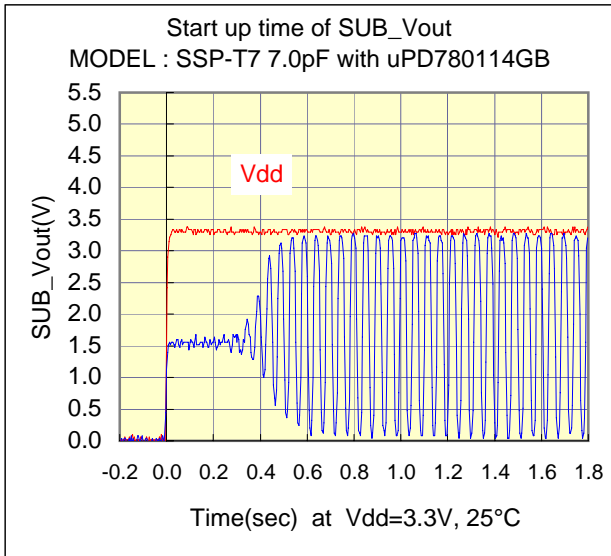
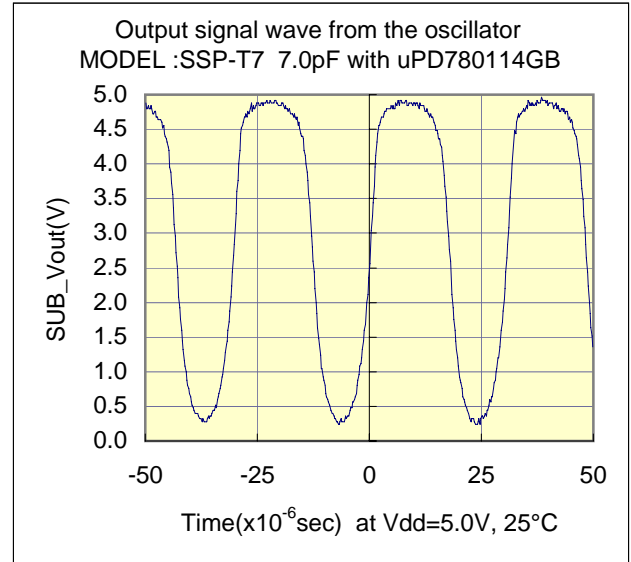
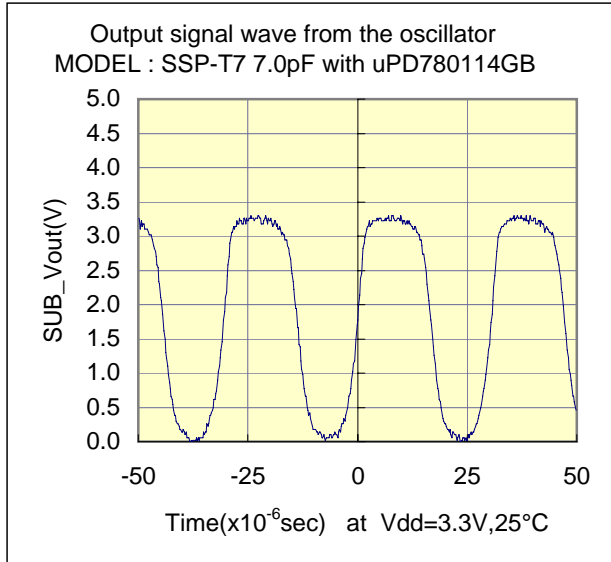
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## Test Data

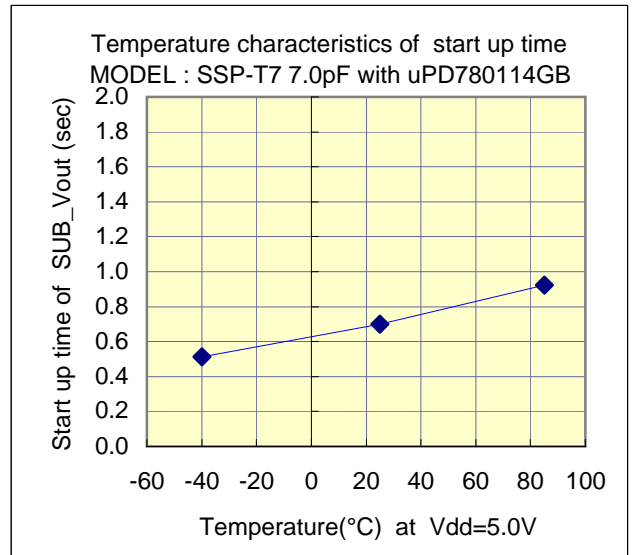
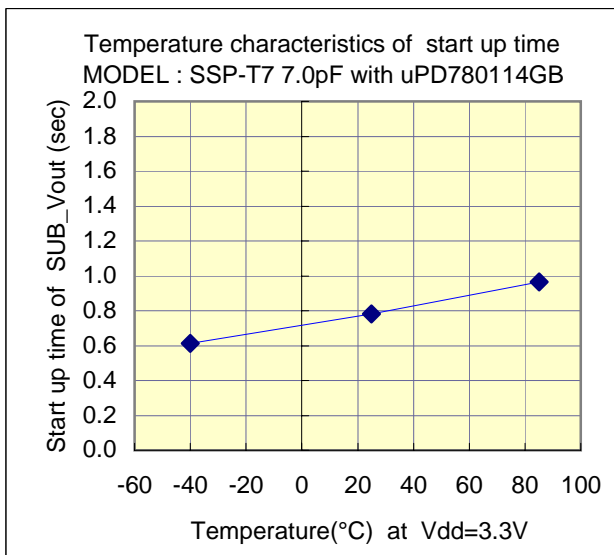
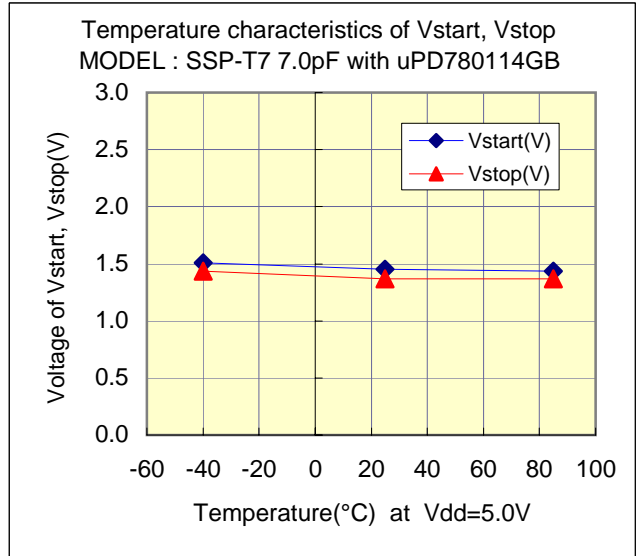
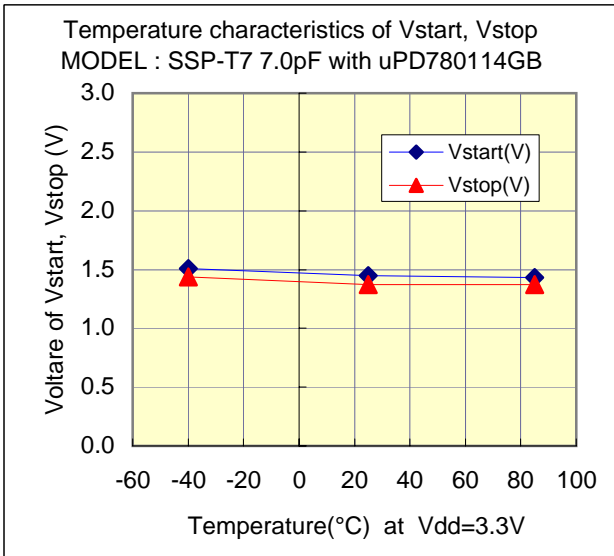
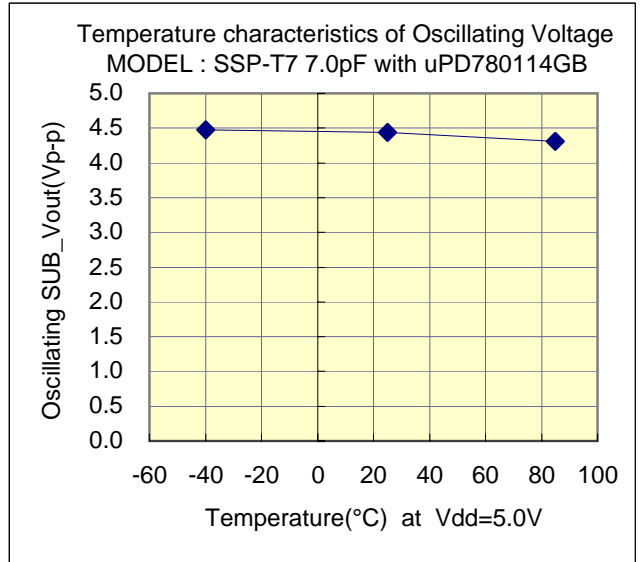
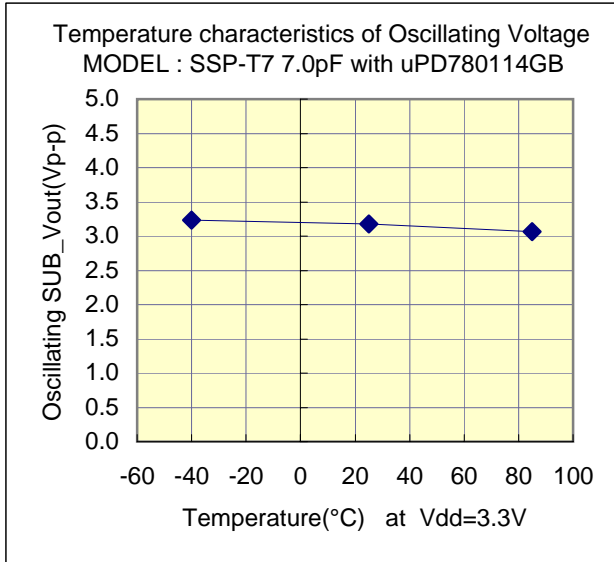


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## Test Data : Temperature characteristics

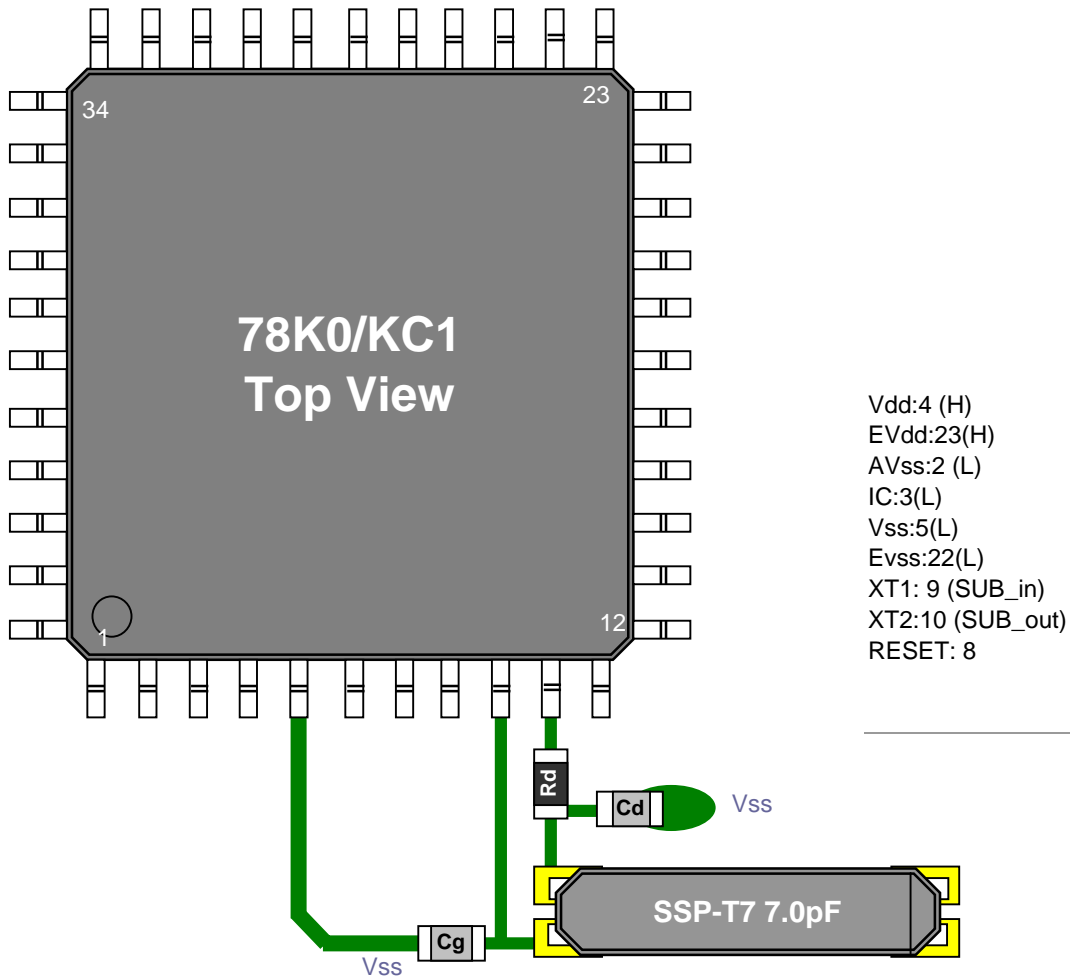


# Evaluation of Subsystem Clock Oscillation Circuit

[ $\mu$ PD780114GB-8ES] LQFP(10x10) 0.8mm pitch

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## Referencial components layout(see Figure 1)

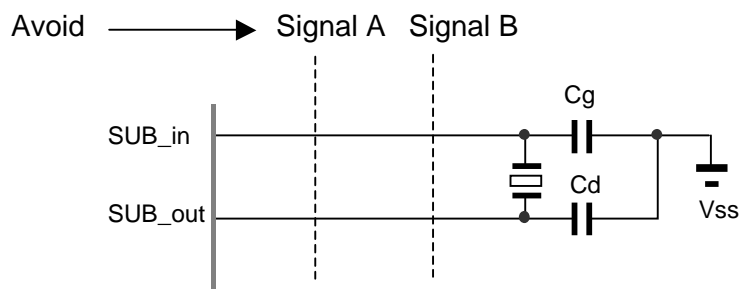


**Figure 1 Referencial components layout**

## Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB\_in and SUB\_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).



**Figure 2 Example of Incorrect Board Design**

**Remak** When using the subsystem clock, insert resistors Rd in series on the SUB\_out side.

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Measurement conditions : 5.0V , 3.3V



## [Evaluation Sample : SSP-T7 7.0pF at 25°C]

SAMPLE	No.	CL(pF)	Fo( Hz )	fr( Hz )	R1( kohm )	Co( pF )	C1( fF )	Q( k )
SSP-T7 7.0pF	1	7	32768.55	32764.38	39.6	0.84	1.994	61.5
	2	7	32767.88	32763.63	39.20	0.85	2.037	60.9
	3	7	32767.83	32763.68	40.30	0.83	1.983	60.8

## [IC Test Data : IC Sampl Rd=220kohm,Cg=9pF,Cd=9pF at 25°C]

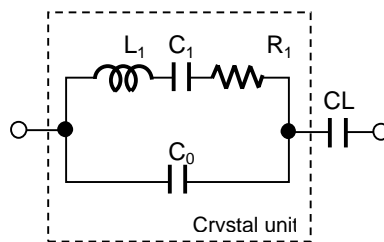
Vdd( V )	IC Sampl	Fosc( Hz )	df / f( x10 <sup>-6</sup> )	DL(x10 <sup>-6</sup> W)	-RL  ( kohm )	Vstart( V )	Ts(sec)
5.0	typ-#01	32768.60	1.53	0.08	869.6	1.45	0.70
	typ-#02	32768.59	1.22	0.08	869.6	1.44	0.70
	typ-#03	32768.61	1.83	0.08	869.6	1.45	0.72

## [IC Test Data : IC Sampl Rd=220kohm,Cg=7pF,Cd=7pF at 25°C]

Vdd( V )	IC Sampl	Fosc( Hz )	df / f( x10 <sup>-6</sup> )	DL(x10 <sup>-6</sup> W)	-RL  ( kohm )	Vstart( V )	Ts(sec)
3.3	typ-#01	32768.63	2.44	0.05	799.6	1.45	0.78
	typ-#02	32768.63	2.29	0.05	799.6	1.44	0.76
	typ-#03	32768.63	2.44	0.05	799.6	1.44	0.78

### Remak ( see figure 3 )

$$F_o = f_r \times \left\{ \frac{C_1}{2 \times (C_o + C_L)} + 1 \right\} \text{ ( Hz )}$$



Fo : Load resonance frequency  
 fr : Resonance frequency  
 R1 : Motional resistance  
 C1 : Motional capacitance  
 Co : Shunt capacitance  
 CL : Load Capacitance

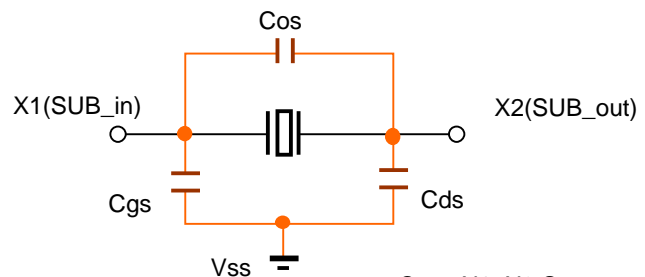
Figure 3 Equivalent circuit of crystal unit, and CL

### Remak ( see figure 4 )

Approximate formula of the load capacitance of the circuit CL.

$$CL = C_g \times C_d / (C_g + C_d) + C_s \text{ ( pF )}$$

Where Cs Stands for stray capacity of the circuit.



Cos : X1\_X2 Stray capacitance  
 Cgs : X1\_Vss Stray capacitance  
 Cds : X2\_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

