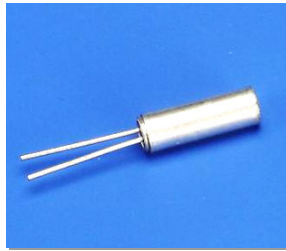


Evaluation of Subsystem Clock Oscillation Circuit

[uPD780138M2GB-8EU] LQFP(10x10) 0.5mm pitch

Measurement conditions : 5.0V (in use of regulator), 5.0V (non use of regulator)

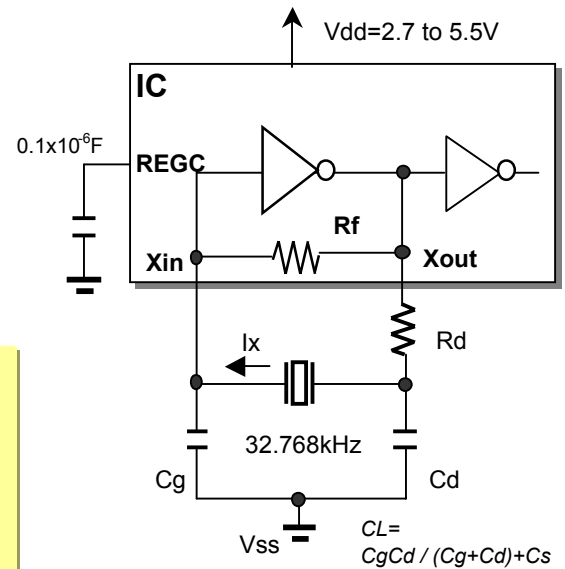
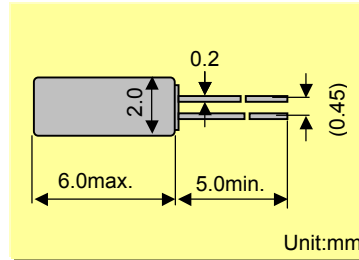


Model	:VT-200
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10 ⁻⁶
Load capacitance	:CL=12.5pF
Equivalent series resistance	:R1=50kohm max
Max. Drive level	:DL=x10 ⁻⁶ W max
Recommended drive level	:DL=0.1x10 ⁻⁶ W typ

FEATURES

- 1.Compact tubular package
- 2.Photolithographic process
- 3.Excellent shock resistance and environmental characteristics.
- 4.Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)



Remark) I_x : current through crystal

When the internal power supply Step-Down circuit is not used, please connect the external power supply to the REGC pin and Vdd pin.

MODEL:VT-200 12.5pF with uPD780138M2GB at 5.0V,25°C

Key specifications	Non use	In use(REG)	Remarks
Current control resistance : Rd (k ohm)	560	330	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	15	15	Optimal capacity in response to CL
Capacitance at drain : Cd (pF)	18	15	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Non use	In use(REG)	Remarks
Matching Accuracy : df / f ($\times 10^{-6}$)	-1.5	1.4	Frequency offset volume at specified Vdd
Voltage Fluctuation : $+/-df / V$ ($\times 10^{-6}$)	1.0	0.0	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL ($\times 10^{-6}$ W)	0.38	0.33	$DL=I_x^2 R_e < 1 \times 10^{-6}$ W, $R_e=R_1(1 + C_o / CL)^2$
Negative resistance : $ -RL $ (kohm)	302	422	5 times larger than R_{1MAX}
Oscillation allowance : M (times)	6.0	8.4	Judgemental standard of oscillation stability
Oscillation start up time : Ts (sec)	1.22	0.80	Time to reach 90% of output level

Temperature characteristics of circuit	Non use	In use(REG)	Remarks
at -40°C Variation : df / T ($\times 10^{-6}$)	-142	-142	Typ.Tp=25°C (K = $-3.5 \times 10^{-8} / ^\circ C^2$)
at +85°C Variation : df / T ($\times 10^{-6}$)	-132	-132	Typ.Tp=25°C (K = $-3.5 \times 10^{-8} / ^\circ C^2$)

The mention value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

Seiko Instruments USA Inc.

2990,West Lomita Blvd., Torrance, CA 90505, U.S.A
 Telephone :+1 310-517-7771 Facsimile :+1 310-517-7792
 Email :crystals@siu-la.com

Seiko Instruments GmbH

Siemensstrasse 9,D-63263 Neu-Isenburg, Germany
 Telephone :+49-6102-297-0 Facsimile :+49-6102-297-320
 Email :info@seiko-instruments.de

Seiko Instruments Inc.

1-8,Nakase,Mihama-ku,Chiba-shi,Chiba 261-8507,Japan
 Facsimile :+81-43-211-8030 E-mail :component@sii.co.jp



We value the "takumi" spirit.

Seiko Instruments Inc.

Phone:+81-43-211-1207(Direct)

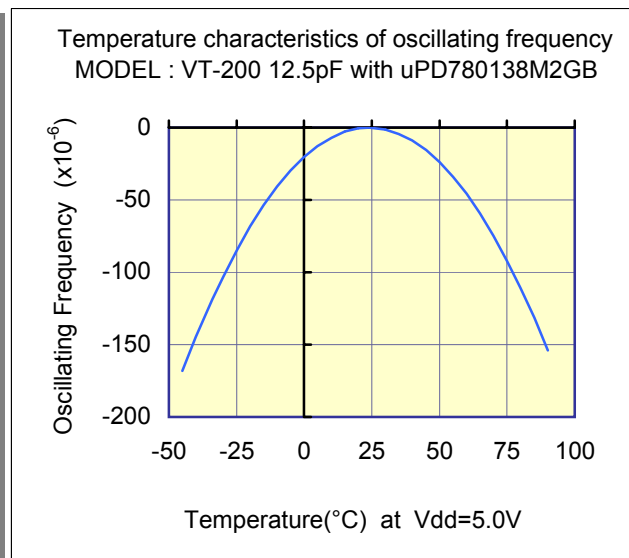
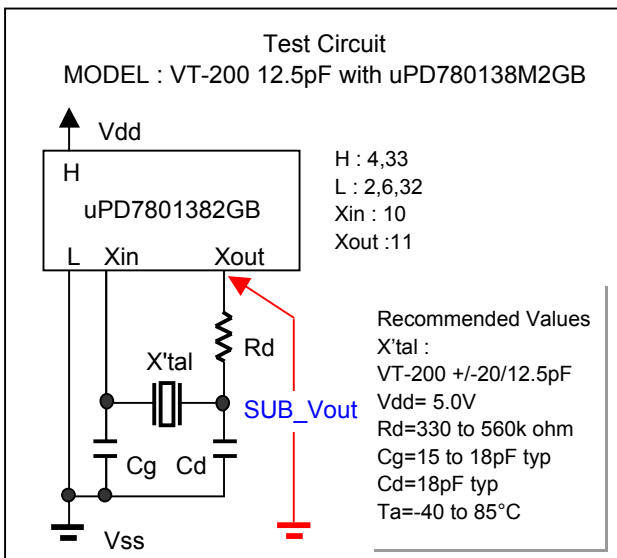
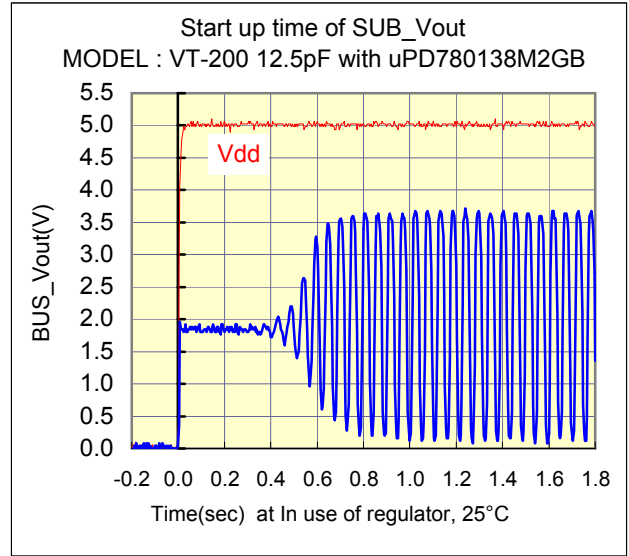
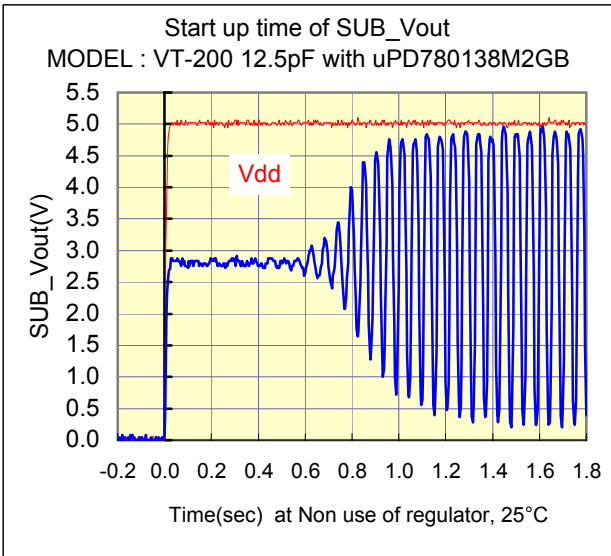
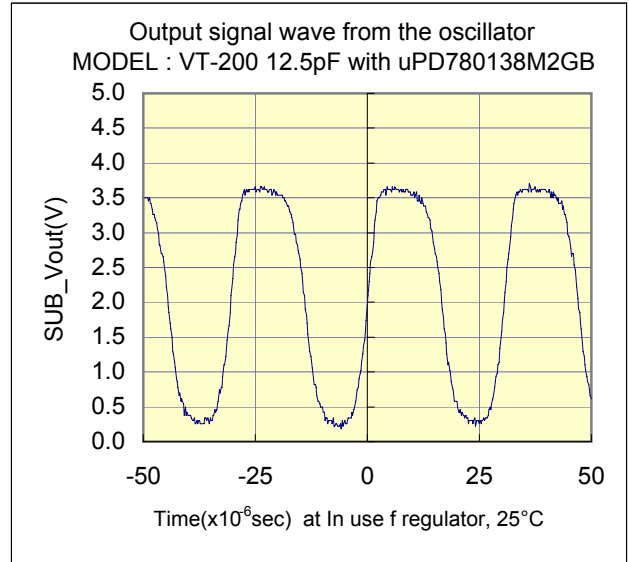
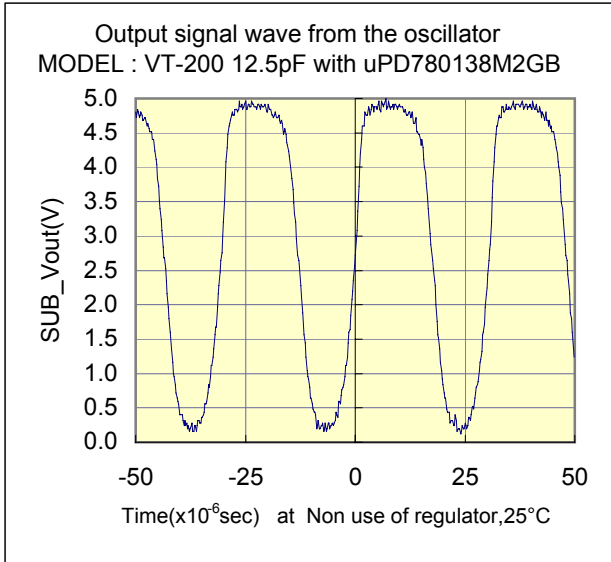
Evaluation of Subsystem Clock Oscillation Circuit

[uPD780138M2GB-8EU] LQFP(10x10) 0.5mm pitch

Measurement conditions : 5.0V (in use of regulator), 5.0V (non use of regulator)



Test Data



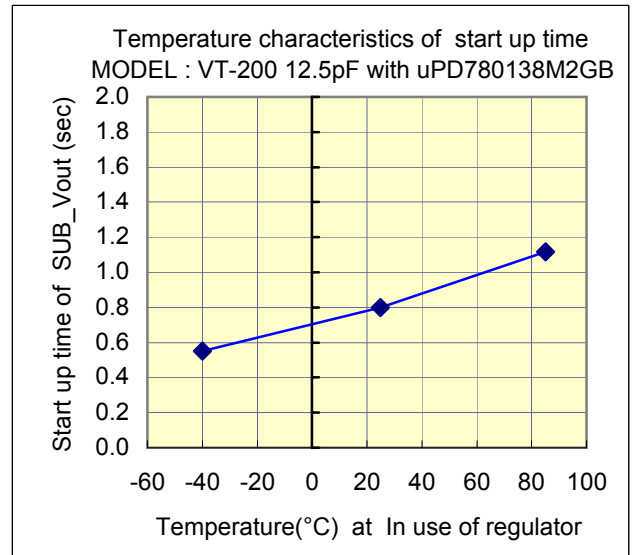
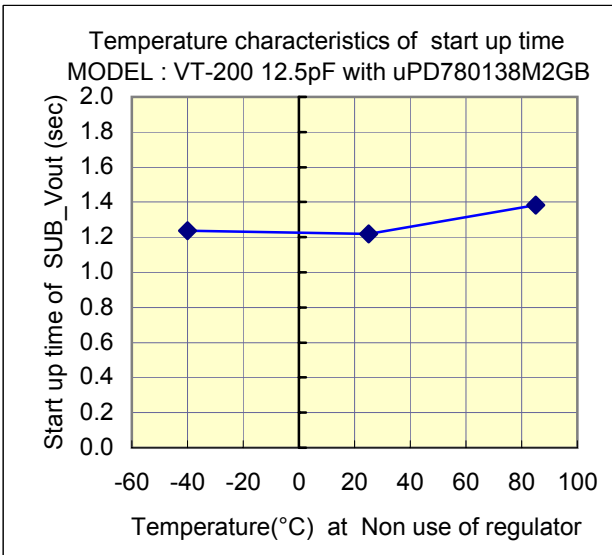
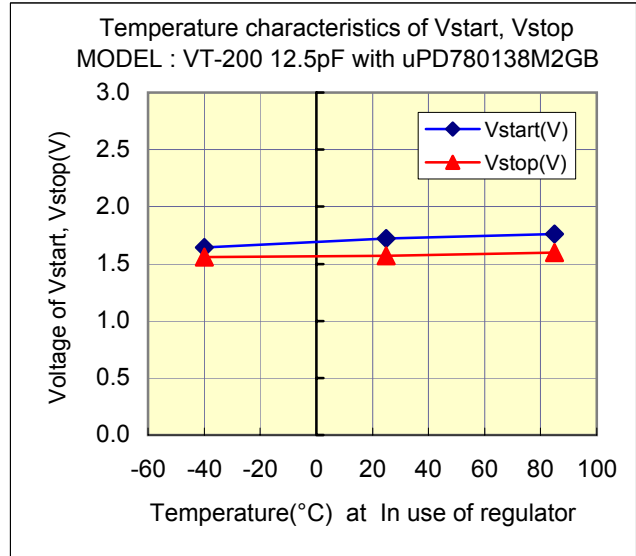
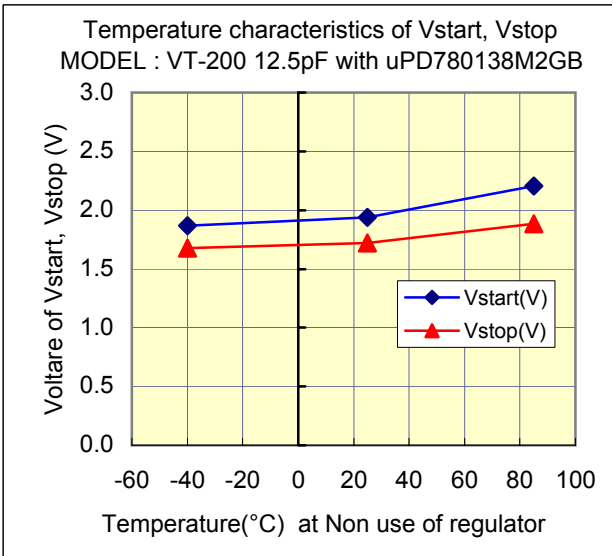
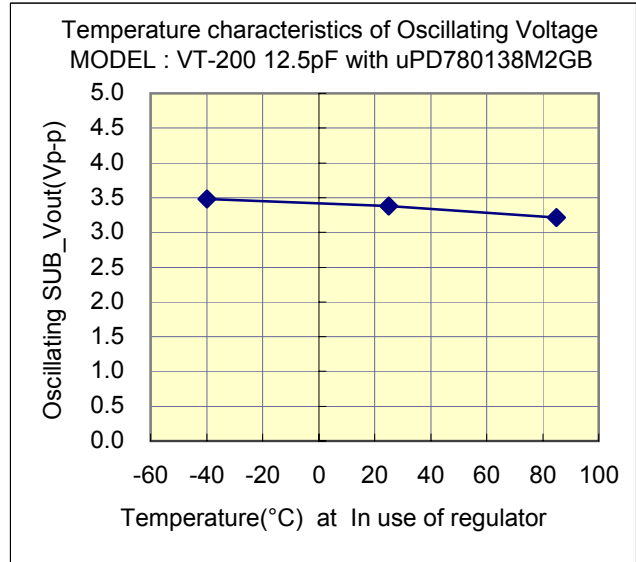
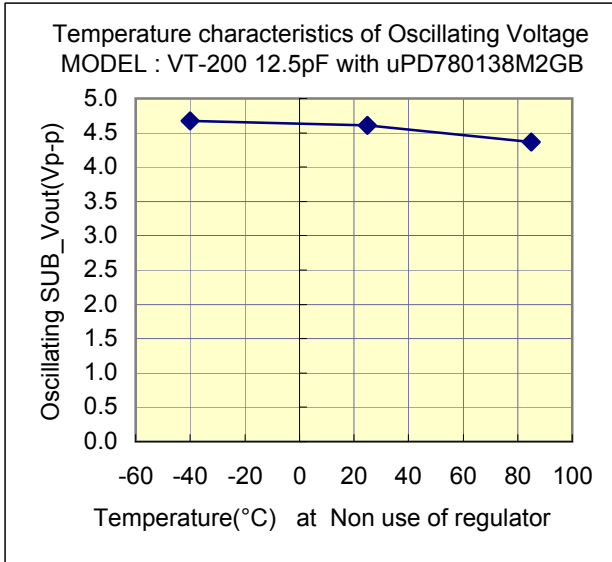
Evaluation of Subsystem Clock Oscillation Circuit

[uPD780138M2GB-8EU] LQFP(10x10) 0.5mm pitch

Measurement conditions : 5.0V (in use of regulator), 5.0V (non use of regulator)



Test Data : Temperature characteristics



Evaluation of Subsystem Clock Oscillation Circuit

[μ PD780138M2GB-8EU] LQFP(10x10) 0.5mm pitch

Measurement conditions : 5.0V (in use of regulator), 5.0V (non use of regulator)



Referencial components layout(see Figure 1)

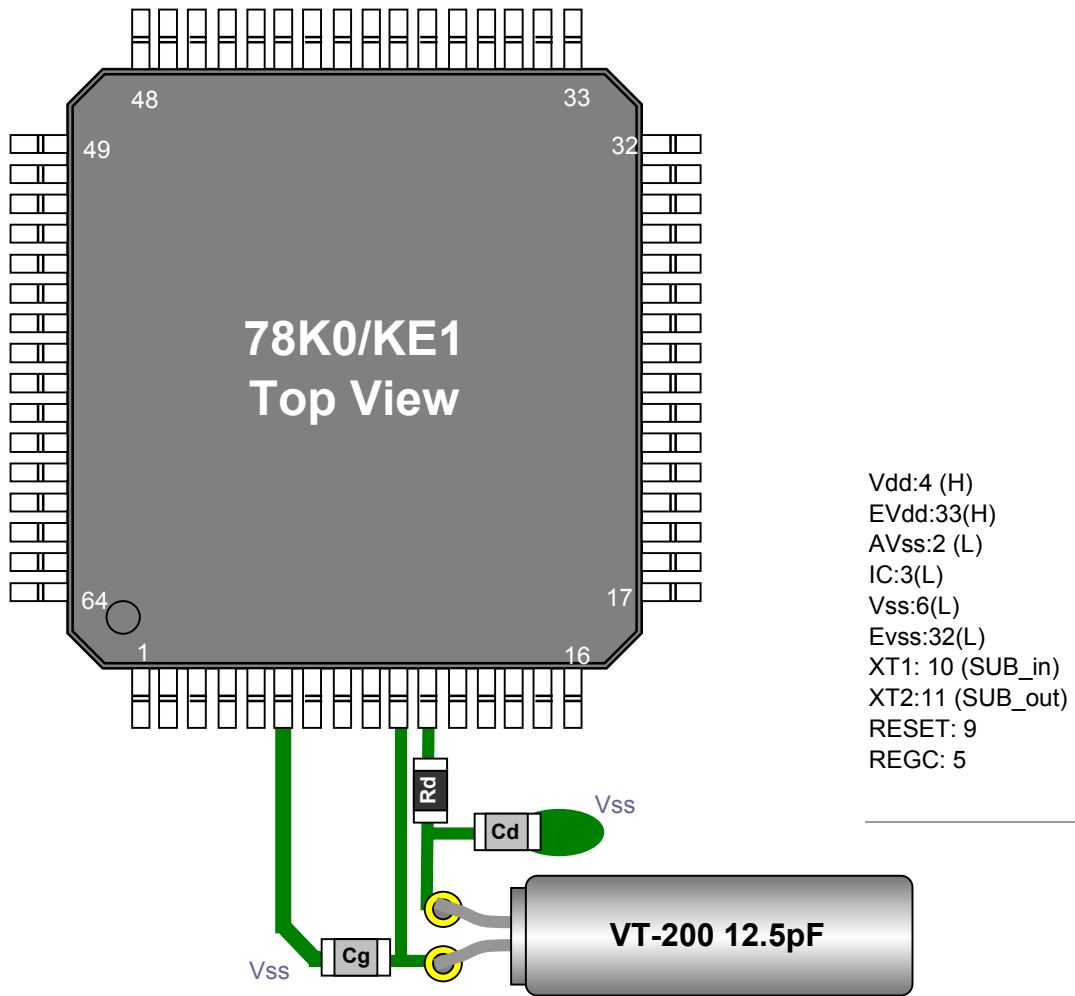


Figure 1 Referencial components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

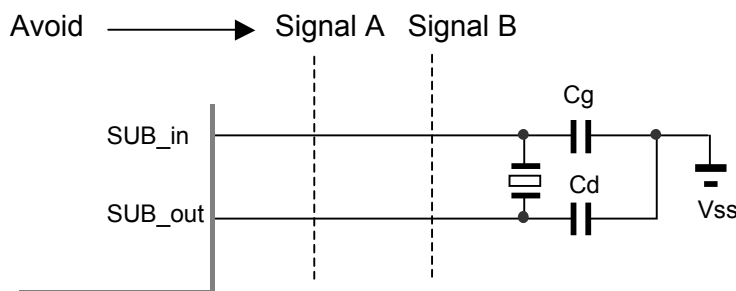


Figure 2 Example of Incorrect Board Design

Remak When using the subsystem clock, insert resistors Rd in series on the SUB_out side.

Evaluation of Subsystem Clock Oscillation Circuit

[uPD780138M2GB-8EU] LQFP(10x10) 0.5mm pitch

Measurement conditions : 5.0V (in use of regulator), 5.0V (non use of regulator)



[Evaluation Sample : VT-200 12.5pF at 25°C]

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
VT-200 12.5pF	1	12.5	32768.11	32765.28	27.4	0.91	2.319	76.5
	2	12.5	32768.09	32765.24	26.9	0.89	2.333	77.4
	3	12.5	32768.34	32765.45	29.9	0.93	2.368	68.6

[IC Test Data : IC Sampl Rd=330k ohm,Cg=18pF,Cd=18pF at 25°C]

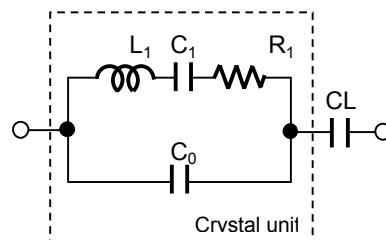
Regulator	IC Sampl	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart(V)	Ts(sec)
In use	typ-#01	32768.16	1.43	0.33	422	1.72	0.80
	typ-#02	32768.16	1.28	0.33	422	1.73	0.85
	typ-#03	32768.15	1.13	0.33	422	1.73	0.83

[IC Test Data : IC Sampl Rd=560k ohm,Cg=15pF,Cd=18pF at 25°C]

Regulator	IC Sampl	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart(V)	Ts(sec)
Non use	typ-#01	32768.07	-1.47	0.38	301.53	1.94	1.22
	typ-#02	32768.07	-1.44	0.40	301.53	1.93	1.14
	typ-#03	32768.06	-1.62	0.37	301.53	1.93	1.00

Remak (see figure 3)

$$F_o = f_r \times \{ C_1 / (2 \times (C_o + C_L) + 1) \} \text{ (Hz)}$$



Fo : Load resonance frequency
fr : Resonance frequency
R1 : Motional resistance
C1 : Motional capacitance
Co : Shunt capacitance
CL : Load Capacitance

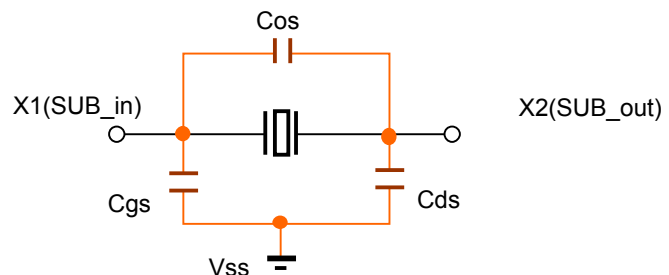
Figure 3 Equivalent circuit of crystal unit, and CL

Remak (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

$$CL = C_g \times C_d / (C_g + C_d) + C_s \text{ (pF)}$$

Where Cs Stands for stray capacity of the circuit.



Cos : X1_X2 Stray capacitance
Cgs : X1_Vss Stray capacitance
Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

