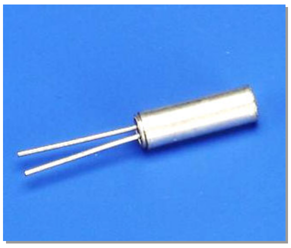
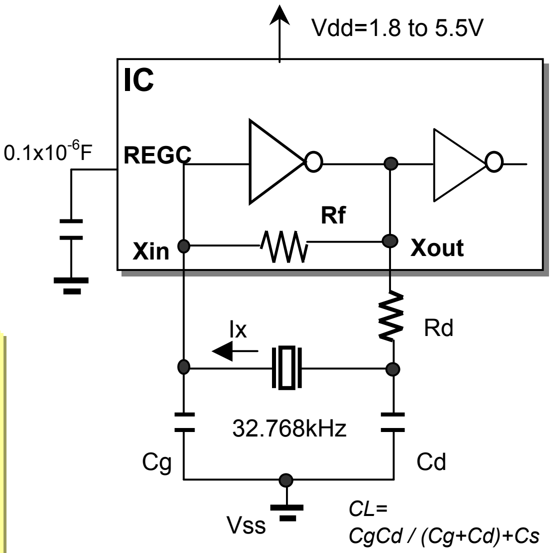
Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0547GC-8BT] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V , 3.3V



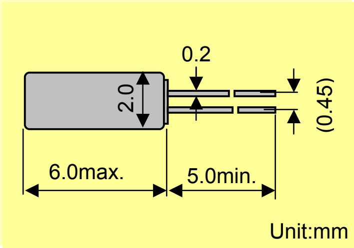
Model	:VT-200
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10^{-6}
Load capacitance	:CL=12.5pF
Equivalent series resistance	:R1=50kohm max
Max. Drive level	:DL=x10^{-6}W max
Recommended drive level	:DL=0.1x10^{-6}W typ



FEATURES

1. Compact tubular package
2. Photolithographic process
3. Excellent shock resistance and environmental characteristics.
4. Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)



Remark) Ix : current through crystal

MODEL:VT-200 12.5pF with uPD78F0547GC at 25°C

Key specifications	Vdd=3.3V	Vdd=5.0V	Remarks
Current control resistance : Rd (k ohm)	100	100	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	15	18	Optimal capacity in response to CL
Capacitance at drain : Cd (pF)	15	15	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vdd=3.3V	Vdd=5.0V	Remarks
Matching Accuracy : df / f (x10^{-6})	-0.3	0.9	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V (x10^{-6})	1.3	1.2	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL (x10^{-6}W)	0.31	0.51	DL=Ix^2 Re < 1x10^{-6}W,Re=R1(1 + Co / CL)^2
Negative resistance : | - RL | (kohm)	271	391	5 times larger than R_{1MAX}
Oscillation allowance : M (times)	5.4	7.8	Judgemental standard of oscillation stability
Voltage of oscillation start : Vstart (V)	1.53	1.53	
Voltage of oscillation stop : Vstop (V)	1.50	1.50	
Oscillation start up time : Ts (sec)	1.03	0.76	Time to reach 90% of output level

Temperature characteristics of circuit		Vdd=3.3V	Vdd=5.0V	Remarks
at -40°C	Variation : df / T (x10^{-6})	-136	-135	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^2)
at +85°C	Variation : df / T (x10^{-6})	-131	-132	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^2)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarante the product's characteristics. Please review and check above parameters at customer's end.

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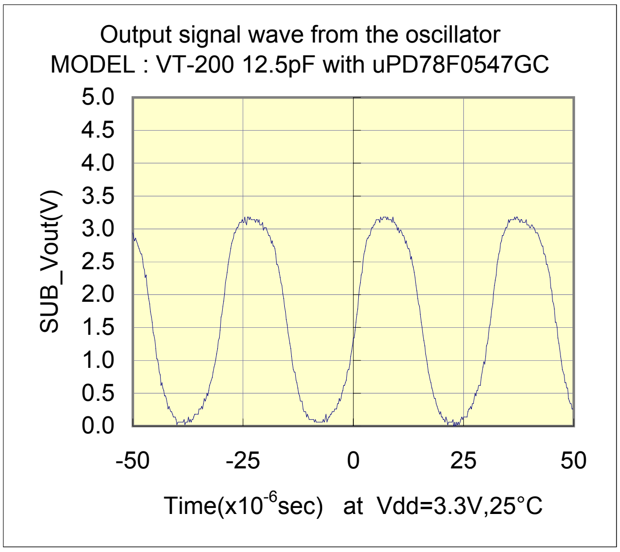
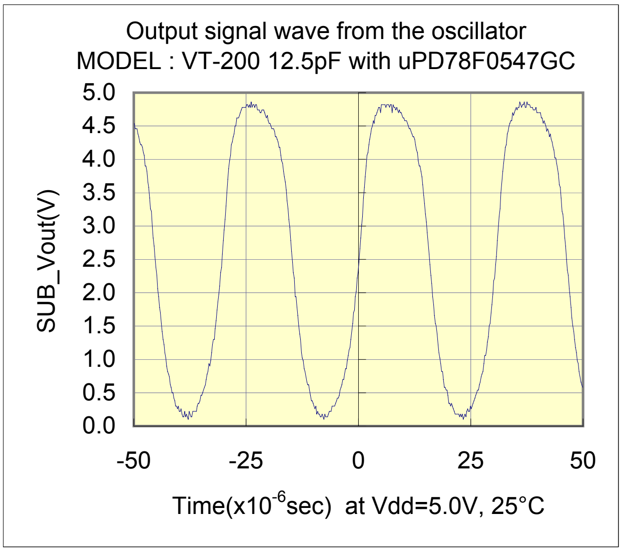
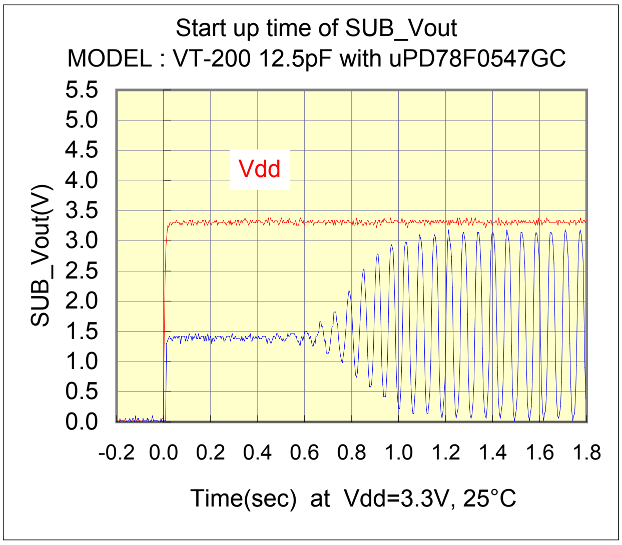
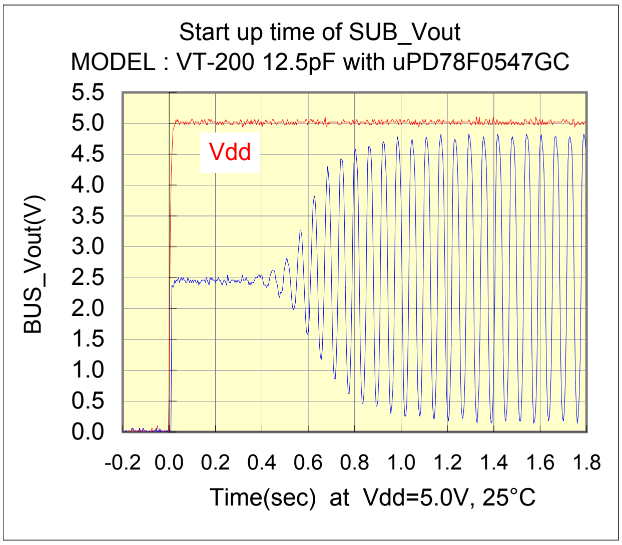
Measurement conditions : 5.0V , 3.3V

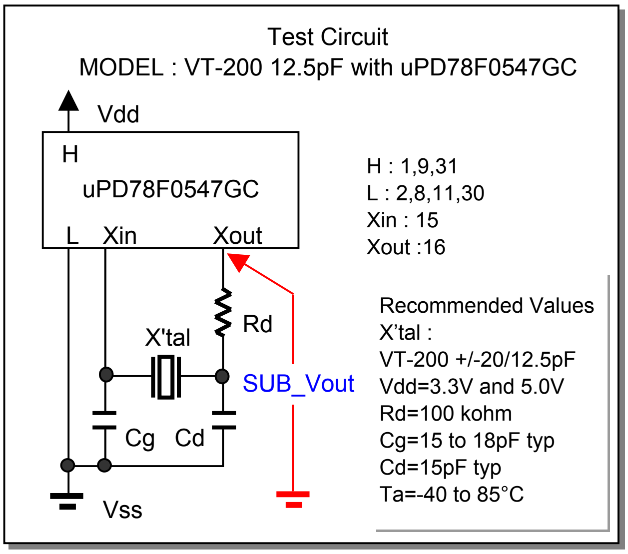
Test Data

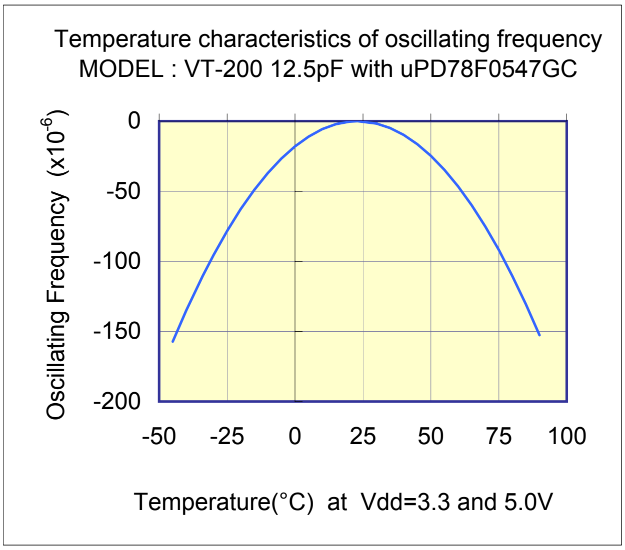










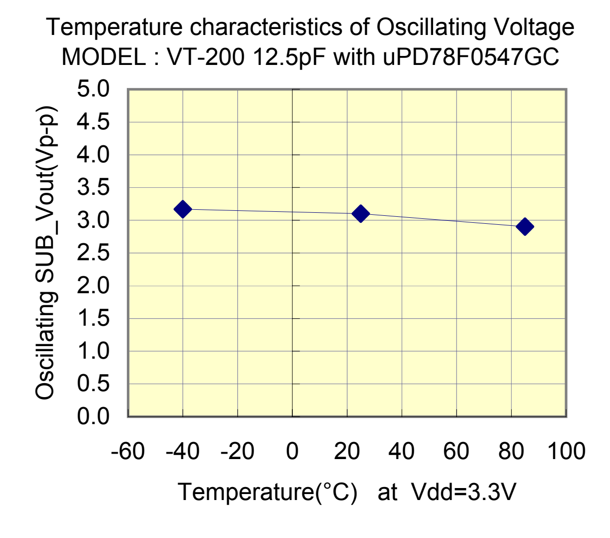


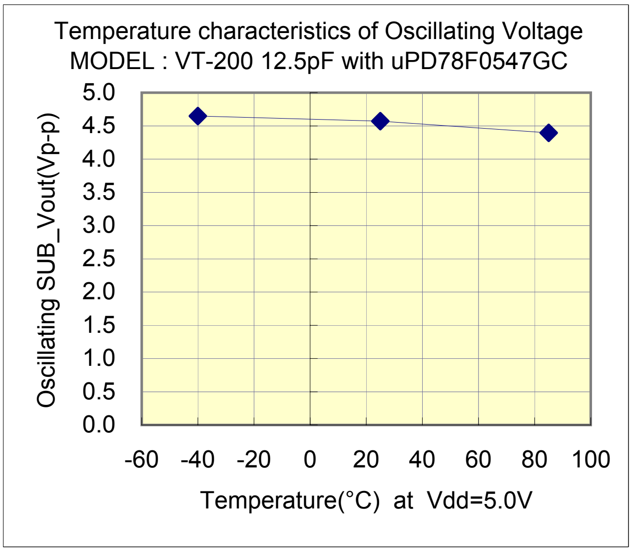
Evaluation of Subsystem Clock Oscillation Circuit

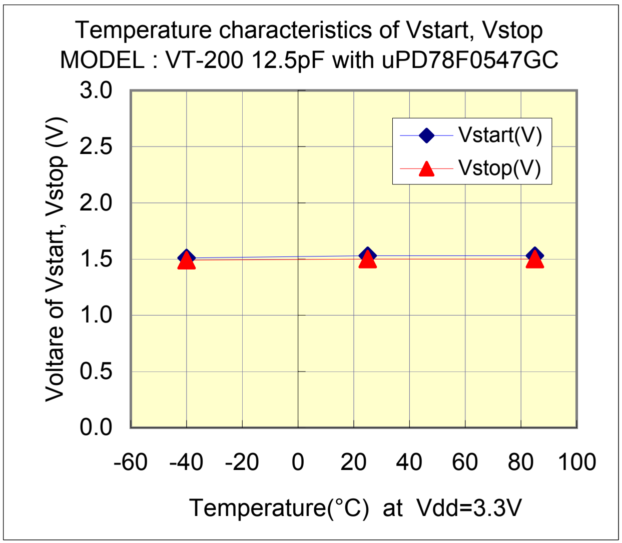
[uPD78F0547GC-8BT] QFP(14x14) 0.65mm pitch
Measurement conditions : 5.0V , 3.3V

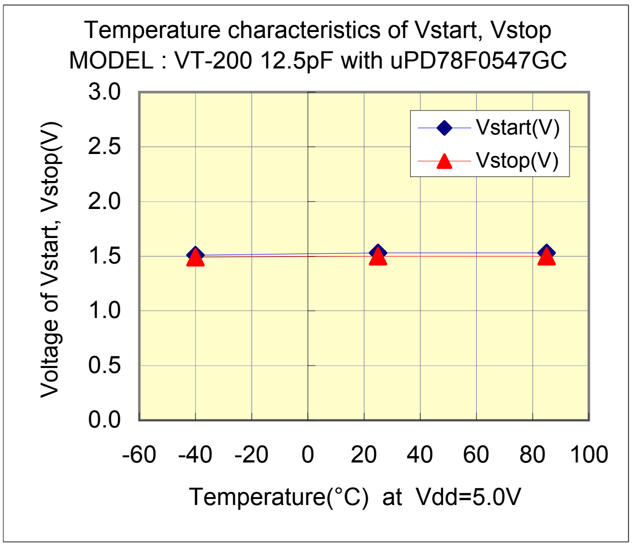
SII

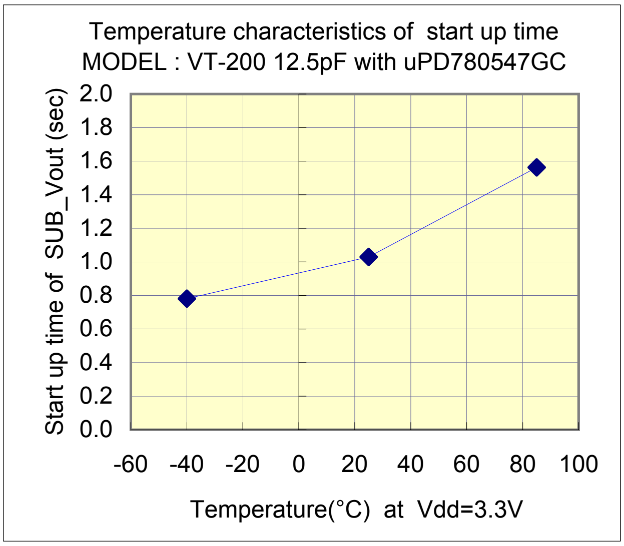
Test Data : Temperature characteristics

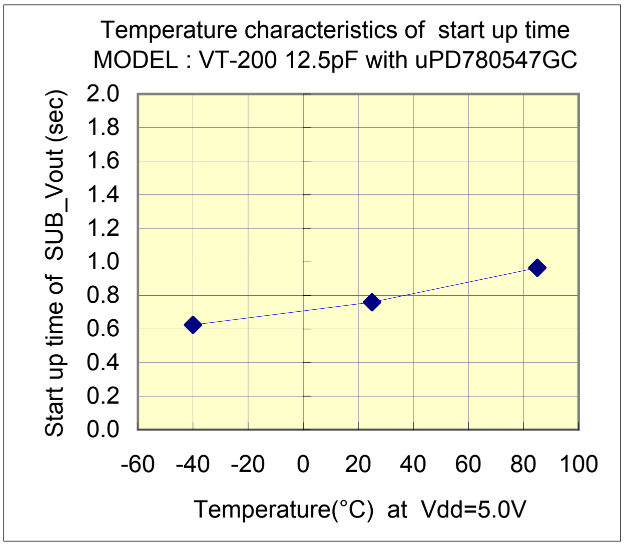












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Measurement conditions : 5.0V , 3.3V

Referential components layout(see Figure 1)

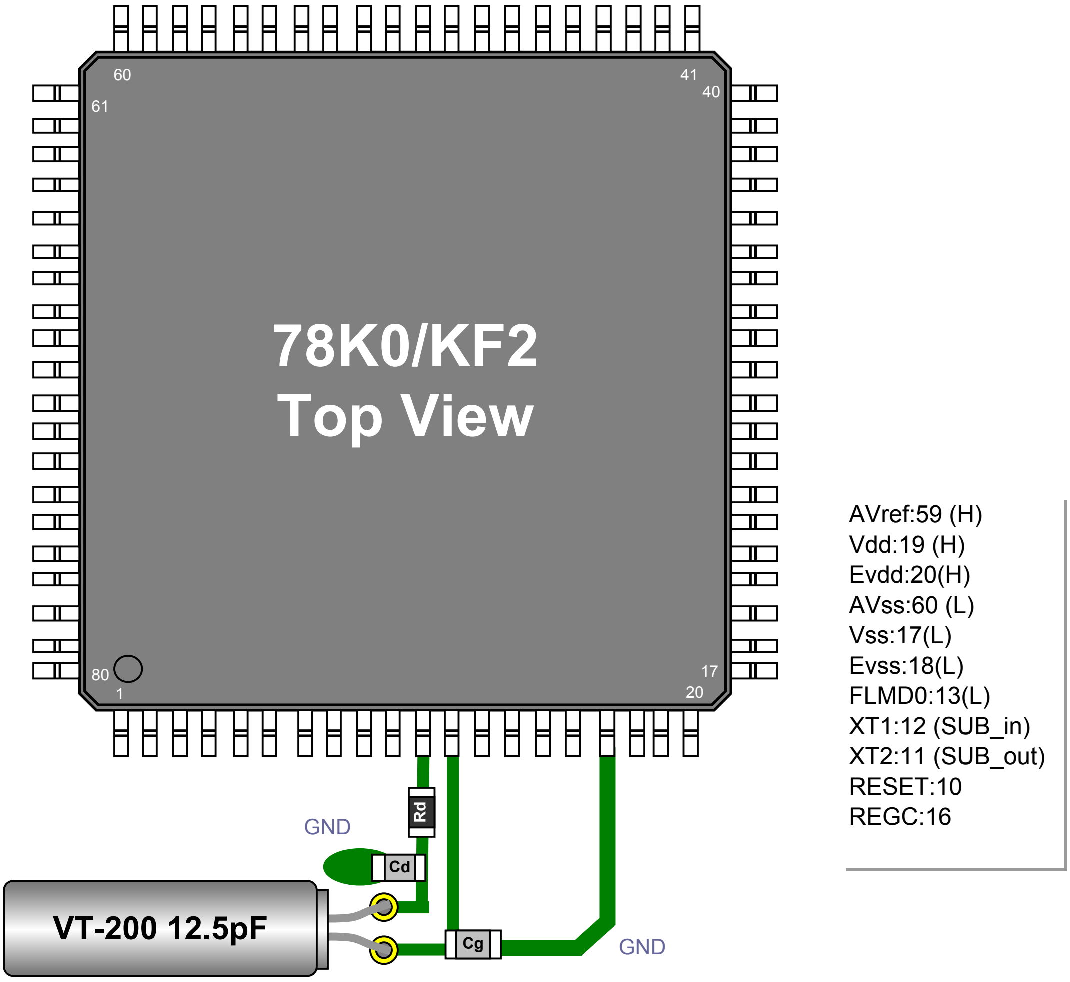

Figure 1 Referential components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.
Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

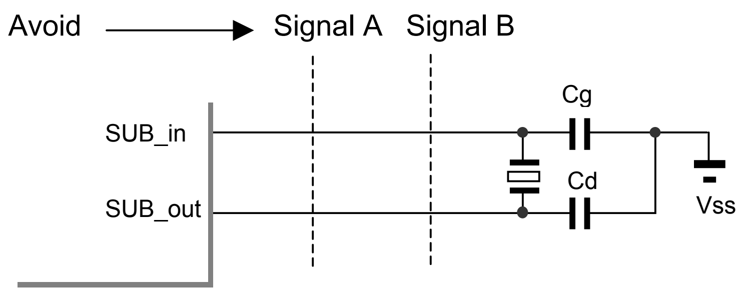

Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert resistors Rd in series on the SUB_out side.

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Measurement conditions : 5.0V , 3.3V

[Evaluation Sample : VT-200 12.5pF at 25°C]

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
VT-200 12.5pF	1	12.5	32768.11	32765.28	27.4	0.91	2.319	76.5
	2	12.5	32768.09	32765.24	26.9	0.89	2.333	77.4
	3	12.5	32768.34	32765.45	29.9	0.93	2.368	68.6

[IC Test Data : IC Sample Rd=100 kohm,Cg=18pF,Cd=15pF at 25°C]

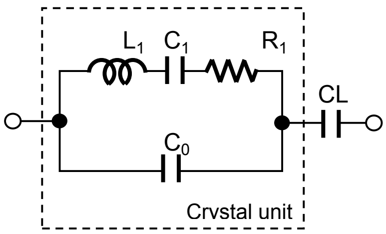
Vdd(V)	IC Sample	Fosc(Hz)	df / f($x10^{-6}$)	DL($x10^{-6}$W)	| -RL |(kohm)	Vstart(V)	Ts(sec)
5.0	CC	32768.14	0.92	0.51	391.47	1.53	0.76
	LLL	32768.16	1.46	0.45	391.47	1.52	0.79
	HLC	32768.13	0.70	0.49	391.47	1.51	0.77
	HHC	32768.10	-0.31	0.56	361.47	1.60	0.82
	HHH	32768.09	-0.73	0.56	361.47	1.58	0.83

[IC Test Data : IC Sample Rd=100 kohm,Cg=15pF,Cd=15pF at 25°C]

Vdd(V)	IC Sample	Fosc(Hz)	df / f($x10^{-6}$)	DL($x10^{-6}$W)	| -RL |(kohm)	Vstart(V)	Ts(sec)
3.3	CC	32768.10	-0.31	0.31	271.47	1.53	1.03
	LLL	32768.10	-0.15	0.27	301.47	1.52	0.97
	HLC	32768.09	-0.67	0.28	301.47	1.51	1.00
	HHC	32768.04	-2.01	0.31	251.47	1.60	1.17
	HHH	32768.04	-2.14	0.31	251.47	1.58	1.20

Remark (see figure 3)

Fo = fr ×{ C1/ (2×(Co + CL) + 1 } (Hz)



Fo : Load resonance frequency

fr : Resonance frequency

R1 : Motional resistance

C1 : Motional capacitance

Co : Shunt capacitance

CL : Load Capacitance

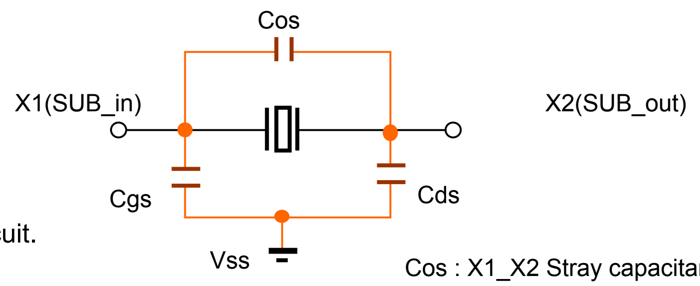
Figure 3 Equivalent circuit of crystal unit, and CL

Remark (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

CL = Cg×Cd / (Cg + Cd) + Cs (pF)

Where Cs Stands for stray capacitance of the circuit.



Cos : X1_X2 Stray capacitance

Cgs : X1_Vss Stray capacitance

Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

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