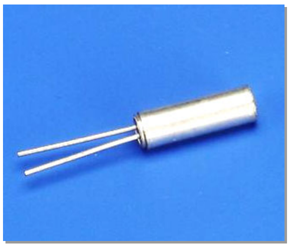
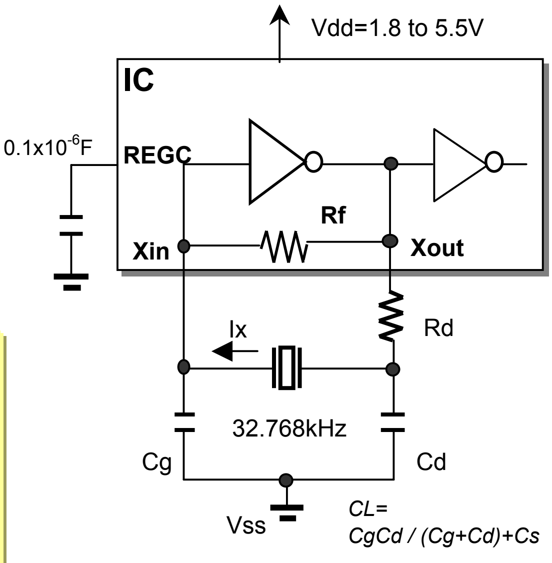
Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0547GC-8BT] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V , 3.3V



Model	:VT-200
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10^{-6}
Load capacitance	:CL=6.0pF
Equivalent series resistance	:R1=50kohm max
Max. Drive level	:DL=x10^{-6}W max
Recommended drive level	:DL=0.1x10^{-6}W typ

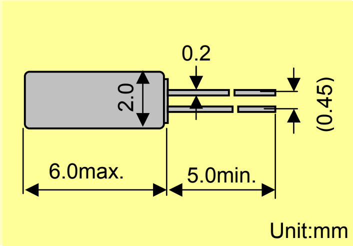


Remark) Ix : current through crystal

FEATURES

1. Compact tubular package
2. Photolithographic process
3. Excellent shock resistance and environmental characteristics.
4. Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)



MODEL:VT-200 6.0pF with uPD78F0547GC at 25°C

Key specifications	Vdd=3.3V	Vdd=5.0V	Remarks
Current control resistance : Rd (k ohm)	100	100	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	4	6	Optimal capacity in response to CL
Capacitance at drain : Cd (pF)	3	5	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vdd=3.3V	Vdd=5.0V	Remarks
Matching Accuracy : df / f (x10^{-6})	1.0	-1.4	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V (x10^{-6})	5.7	7.2	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL (x10^{-6}W)	0.02	0.04	DL=Ix^2 Re < 1x10^{-6}W,Re=R1(1 + Co / CL $)^2$
Negative resistance : | - RL | (kohm)	549	659	5 times larger than R_{1MAX}
Oscillation allowance : M (times)	11.0	13.2	Judgemental standard of oscillation stability
Voltage of oscillation start : Vstart (V)	1.52	1.52	
Voltage of oscillation stop : Vstop (V)	1.50	1.50	
Oscillation start up time : Ts (sec)	0.74	0.67	Time to reach 90% of output level

Temperature characteristics of circuit		Vdd=3.3V	Vdd=5.0V	Remarks
at -40°C	Variation : df / T (x10^{-6})	-129	-130	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^2)
at +85°C	Variation : df / T (x10^{-6})	-138	-139	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^2)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarante the product's characteristics. Please review and check above parameters at customer's end.

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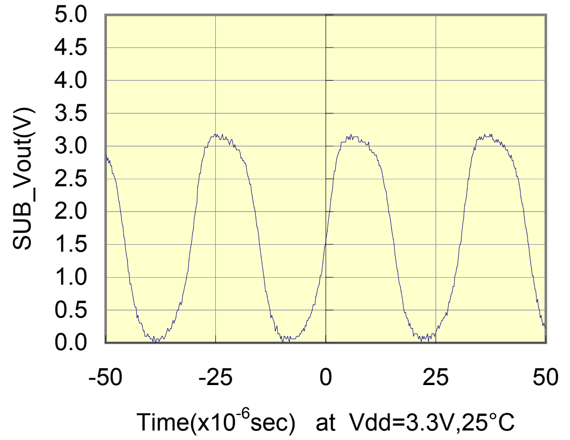
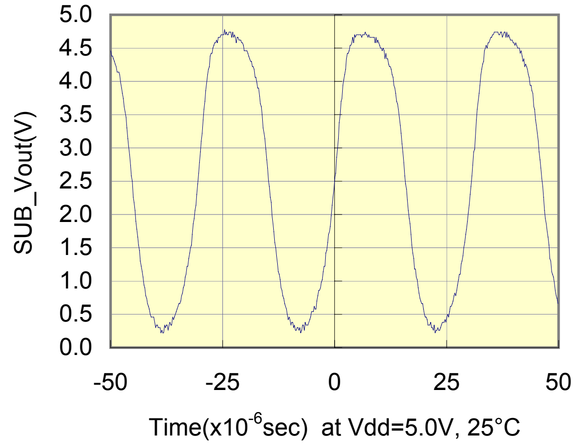
Measurement conditions : 5.0V , 3.3V

Test Data

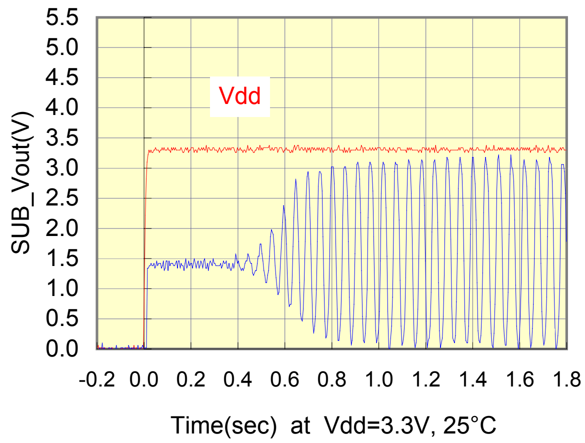
Output signal wave from the oscillator
MODEL : VT-200 6.0pF with uPD78F0547GC



Output signal wave from the oscillator
MODEL : VT-200 6.0pF with uPD78F0547GC



Start up time of SUB_Vout
MODEL : VT-200 6.0pF with uPD78F0547GC



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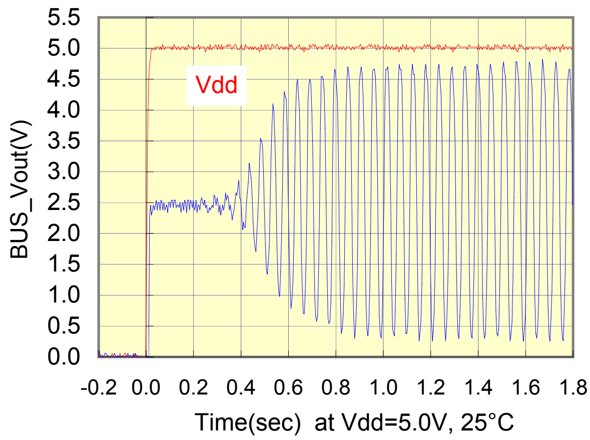
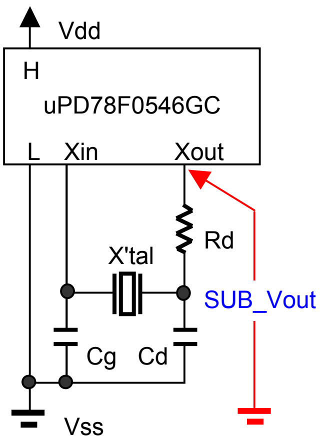


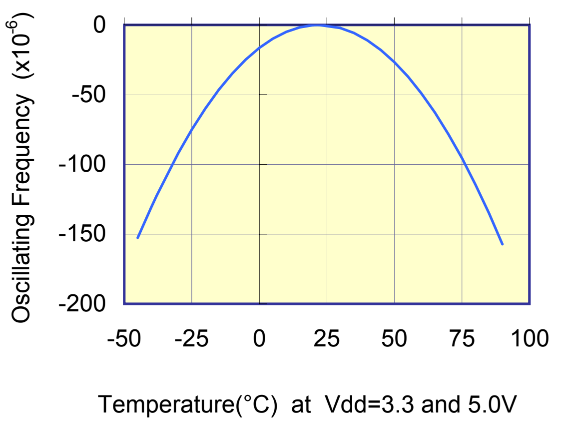
Test Circuit
MODEL : VT-200 6.0pF with uPD78F0547GC



H : 19,20,59
L : 13,17,18,50
Xin : 12
Xout :11

Recommended Values
X'tal :
VT-200 +/-20/6.0pF
Vdd=3.3V and 5.0V
Rd=100 kohm
Cg= 4 to 6pF typ
Cd= 3 to 5pF typ
Ta=-40 to 85°C

Temperature characteristics of oscillating frequency
MODEL : VT-200 6.0pF with uPD78F0547GC



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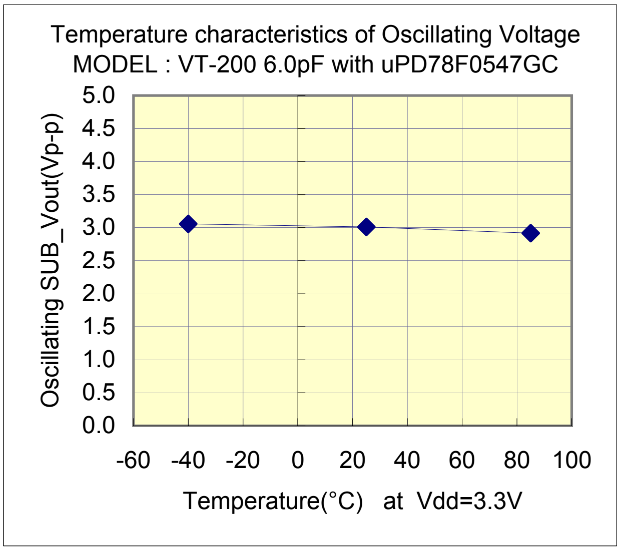
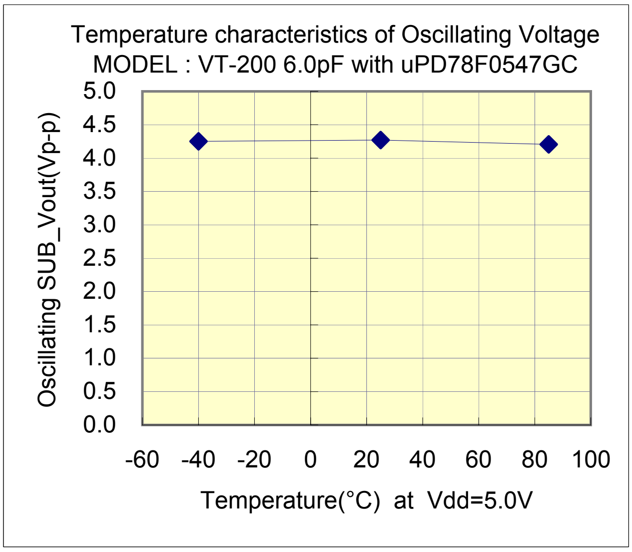
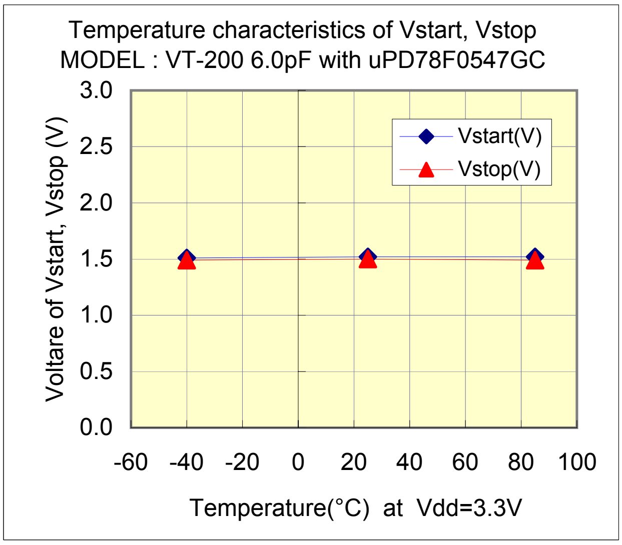
[uPD78F0547GC-8BT] QFP(14x14) 0.65mm pitch

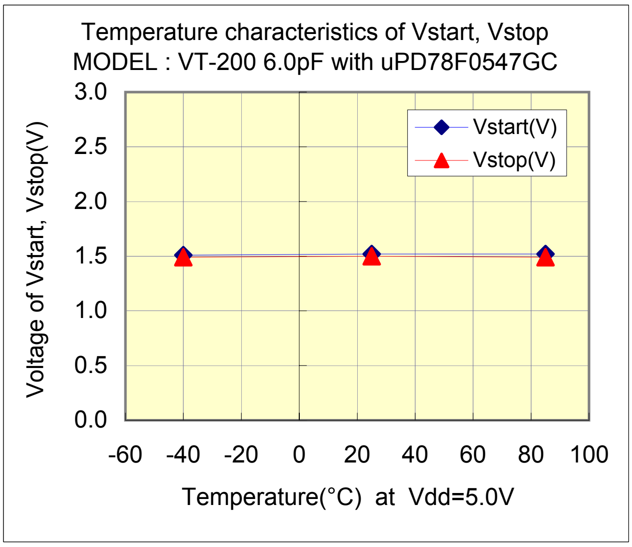
Measurement conditions : 5.0V , 3.3V

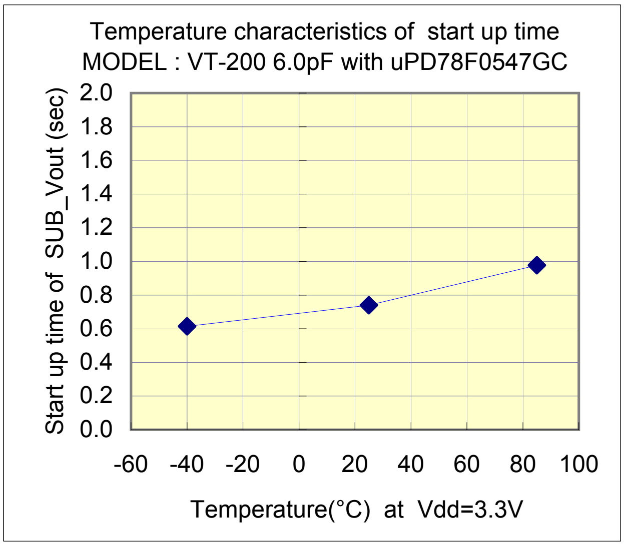
Test Data : Temperature characteristics

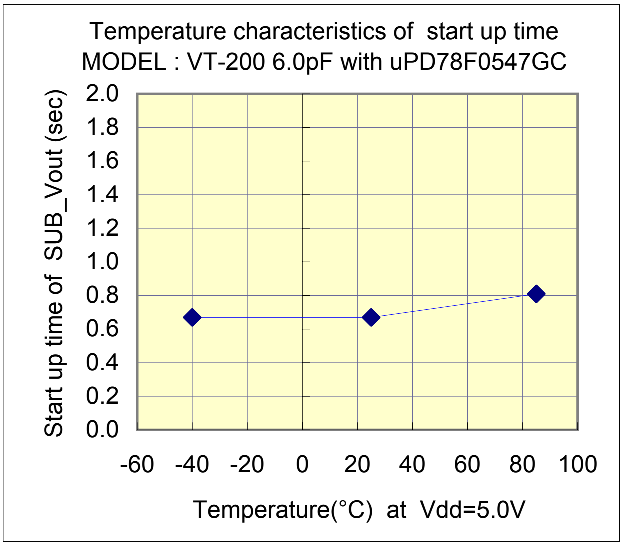












Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0547GC-8BT] QFP(14x14) 0.65mm pitch

Measurement conditions : 5.0V , 3.3V

Referential components layout(see Figure 1)

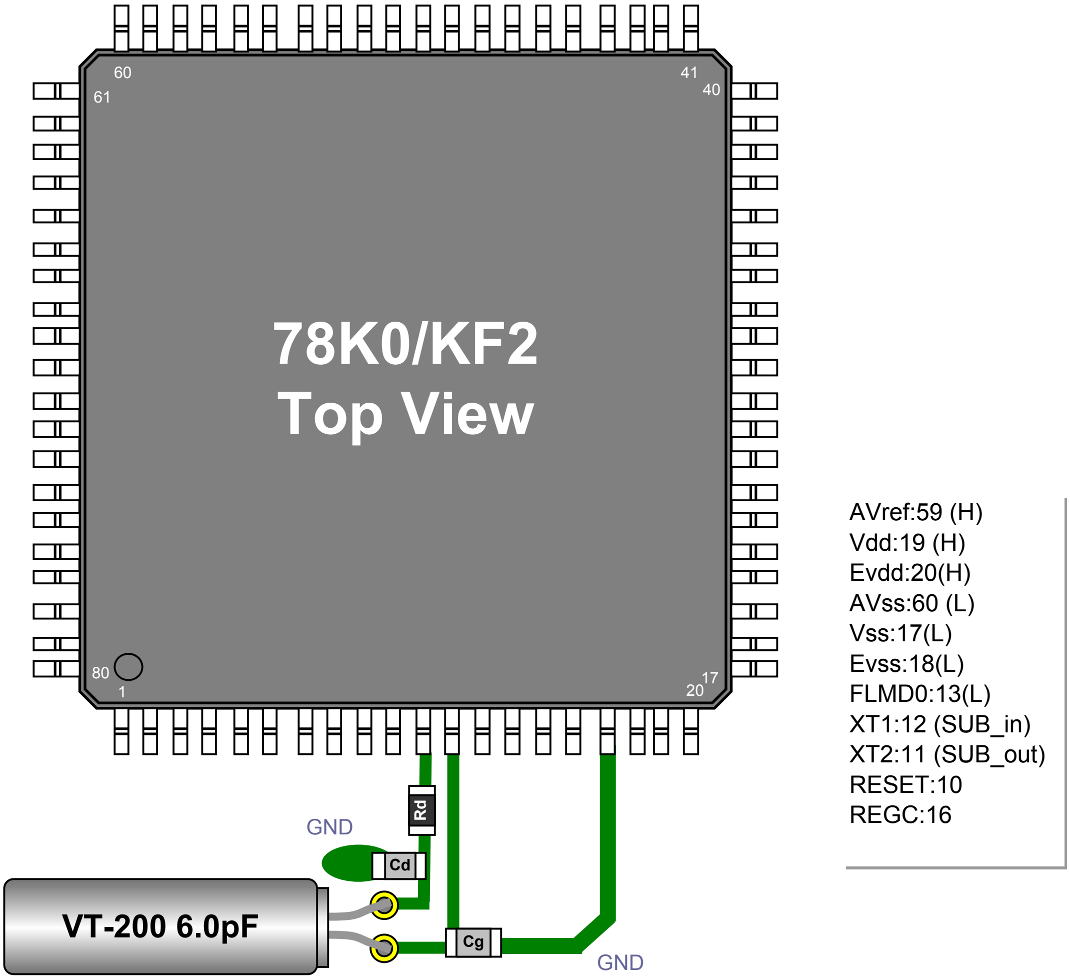


Figure 1 Referential components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.
Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

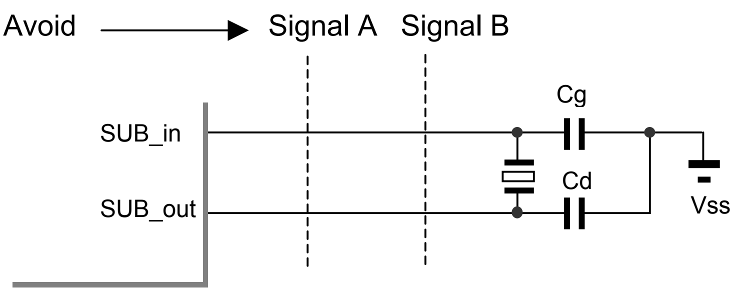


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert resistors Rd in series on the SUB_out side.

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SII

[Evaluation Sample : VT-200 6.0pF at 25°C]

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
VT-200 6.0pF	1	6	32768.18	32762.98	28.7	0.91	2.193	77.2
	2	6	32768.18	32763.04	27.8	0.89	2.161	80.9
	3	6	32768.19	32763.00	27.2	0.90	2.187	81.7

[IC Test Data : IC Sample Rd=100 kohm,Cg=6pF,Cd=5pF at 25°C]

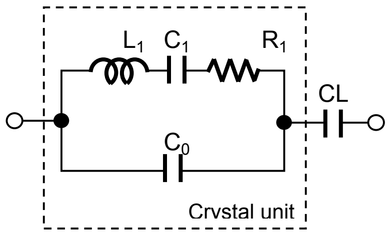
Vcc(V)	IC Sample	Fosc(Hz)	df / f($x10^{-6}$)	DL($x10^{-6}$W)	|-RL|(kohm)	Vstart(V)	Ts(sec)
5.0	CC	32768.13	-1.43	0.04	659.14	1.52	0.67
	LLL	32768.06	-3.66	0.03	599.14	1.51	0.73
	HLC	32768.13	-1.68	0.04	659.14	1.51	0.63
	HHC	32767.96	-6.65	0.06	599.14	1.54	0.66
	HHH	32767.93	-7.63	0.06	659.14	1.54	0.67

[IC Test Data : IC Sample Rd=100 kohm,Cg=4pF,Cd=3pF at 25°C]

Vcc(V)	IC Sample	Fosc(Hz)	df / f($x10^{-6}$)	DL($x10^{-6}$W)	|-RL|(kohm)	Vstart(V)	Ts(sec)
3.3	CC	32768.21	0.98	0.02	549.14	1.52	0.74
	LLL	32768.15	-1.07	0.02	509.14	1.51	0.79
	HLC	32768.06	-3.66	0.02	509.14	1.51	0.75
	HHC	32767.92	-8.00	0.03	469.14	1.54	0.83
	HHH	32767.90	-8.54	0.03	469.14	1.53	0.83

Remark (see figure 3)

$Fo = fr \times \{ C1 / (2 \times (Co + CL) + 1 \}$ (Hz)



Fo : Load resonance frequency
fr : Resonance frequency
R1 : Motional resistance
C1 : Motional capacitance
Co : Shunt capacitance
CL : Load Capacitance

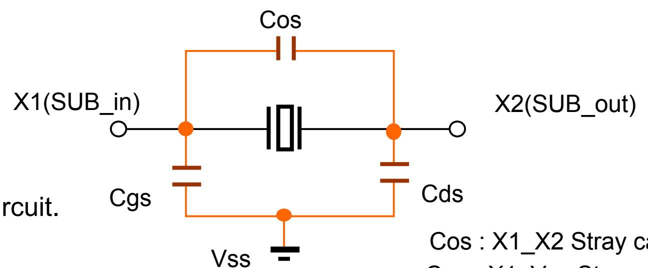
Figure 3 Equivalent circuit of crystal unit, and CL

Remark (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

$$CL = Cg \times Cd / (Cg + Cd) + Cs \ \ (pF)$$

Where Cs Stands for stray capacitance of the circuit.



Cos : X1_X2 Stray capacitance
Cgs : X1_Vss Stray capacitance
Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

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