

Evaluation of Subsystem Clock Oscillation Circuit

[M38C59MCHP-80P] LQFP(12x12) 0.5mm pitch

Measurement conditions :3.3V, 5.0V

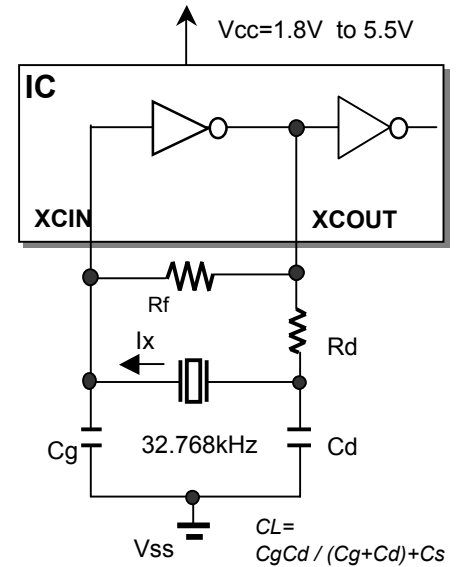
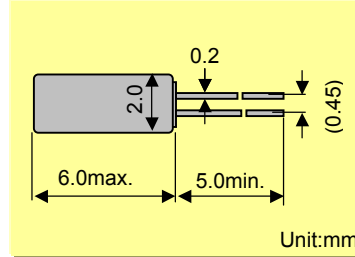


Model	:VT-200
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10 ⁶
Load capacitance	:CL=6.0pF
Equivalent series resistance	:R1=50kohm max
Max. drive level	:DL=1x10 ⁶ W max
Level of drive	:DL=0.1x10 ⁶ W typ

FEATURES

- 1.Compact tubular package
- 2.Photolithographic process
- 3.Excellent shock resistance and environmental characteristics.
- 4.Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)



MODEL:VT-200 6.0pF with M38C59MCHP at 25°C

Key specifications	Vcc=3.3V	Vcc=5.0V	Remarks
Negative feedback resistance : Rf (M ohm)	10	10	
Current control resistance : Rd (k ohm)	330	330	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	4	4	Optimal capacity in response to CL
Capacitance at drain : Cd (pF)	5	5	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vcc=3.3V	Vcc=5.0V	Remarks
Matching Accuracy : df / f (x10 ⁻⁶)	-2.8	2.4	Frequency offset volume at specified Vdd
Voltage Fluctuation : $+/-df / V$ (x10 ⁻⁶)	1.3	1.1	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL (x10 ⁻⁶ W)	0.01	0.01	$DL=I_x^2 R_e < 1 \times 10^{-6} W, R_e=R_1(1 + C_o / CL)^2$
Negative resistance : $ -RL $ (kohm)	507	467	5 times larger than R _{1MAX}
Oscillation allowance : M (times)	10.1	9.3	Judgemental standard of oscillation stability
Voltage of oscillation start : Vstart (V)	1.80	1.80	
Voltage of oscillation stop : Vstop (V)	1.65	1.65	
Oscillation start up time : Ts (sec)	0.56	0.60	Time to reach 90% of output level

Temperature characteristics of circuit		Vcc=3.3V	Vcc=5.0V	Remarks
at -20°C	Variation : df / T (x10 ⁻⁶)	-57	-58	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)
at +85°C	Variation : df / T (x10 ⁻⁶)	-144	-143	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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We value the "takumi" spirit.

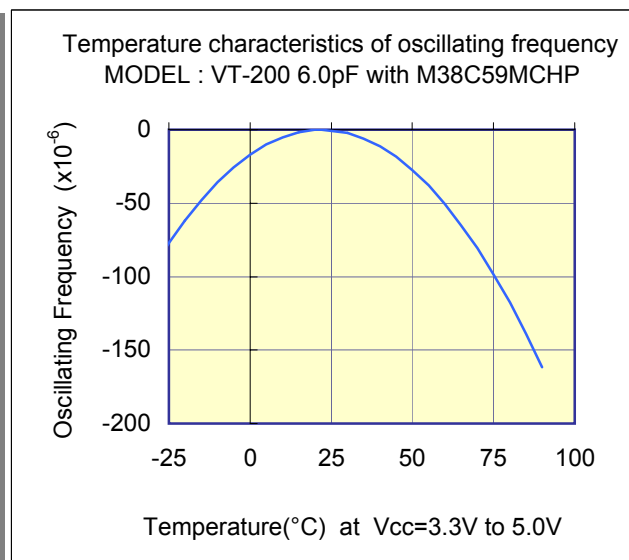
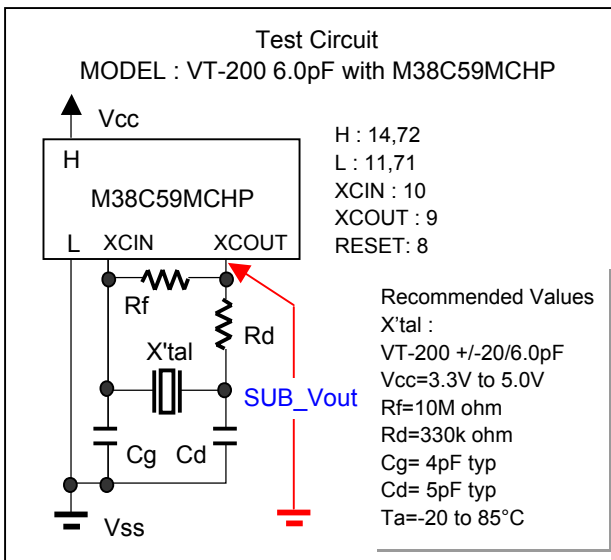
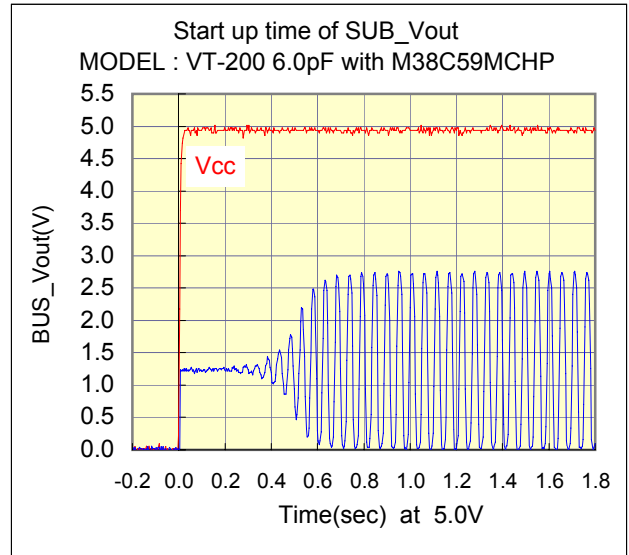
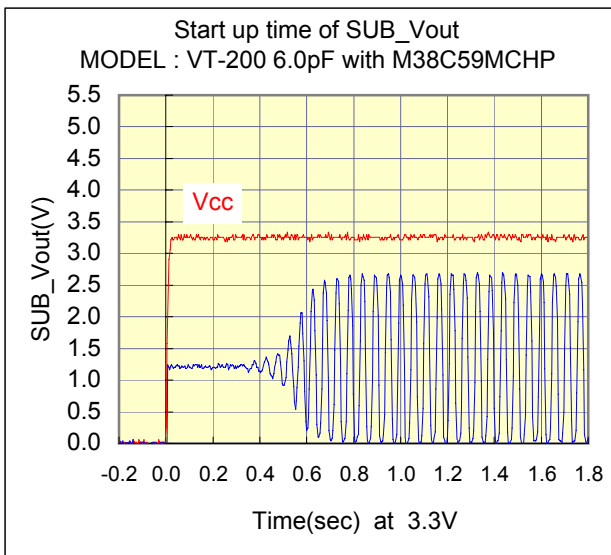
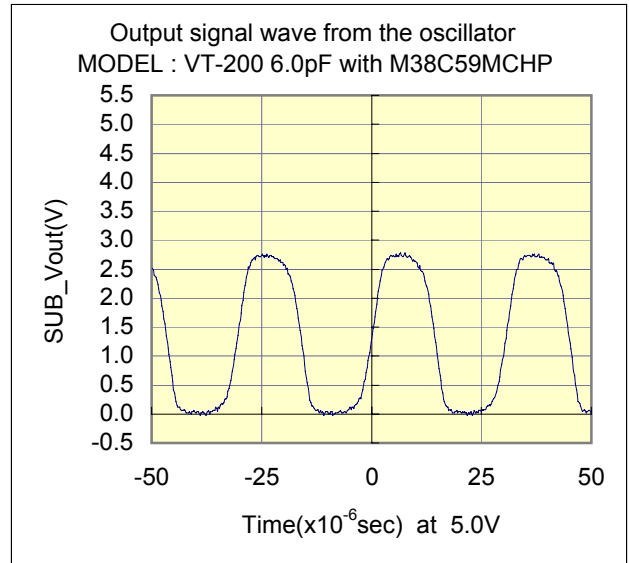
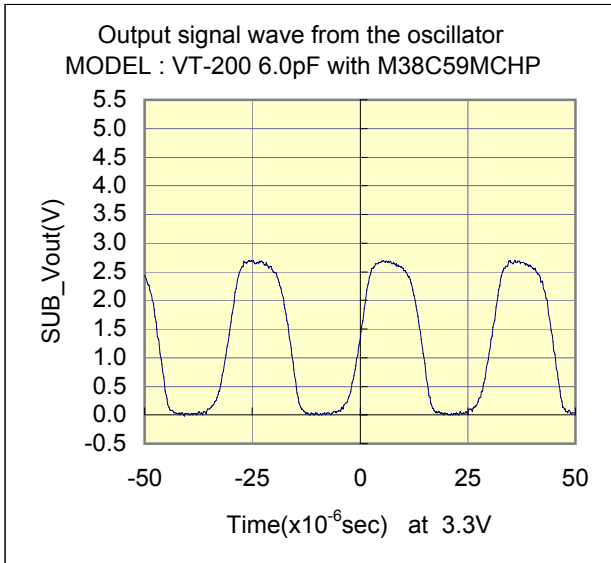
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Test Data at 25°C

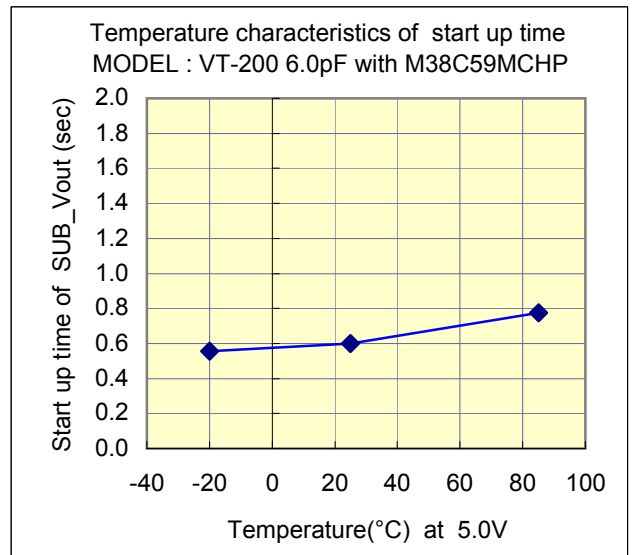
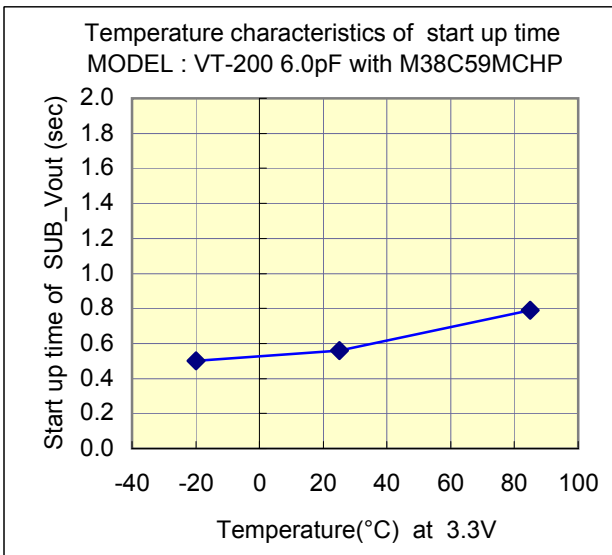
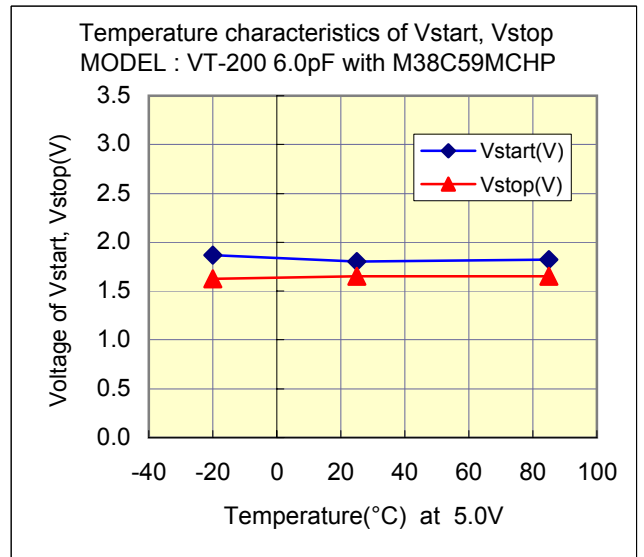
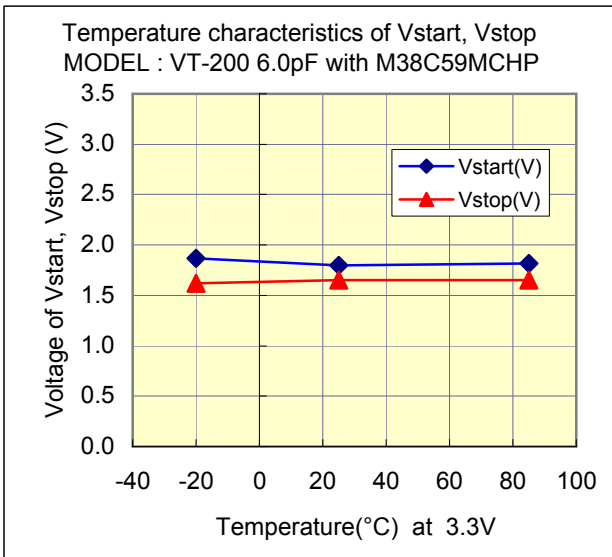
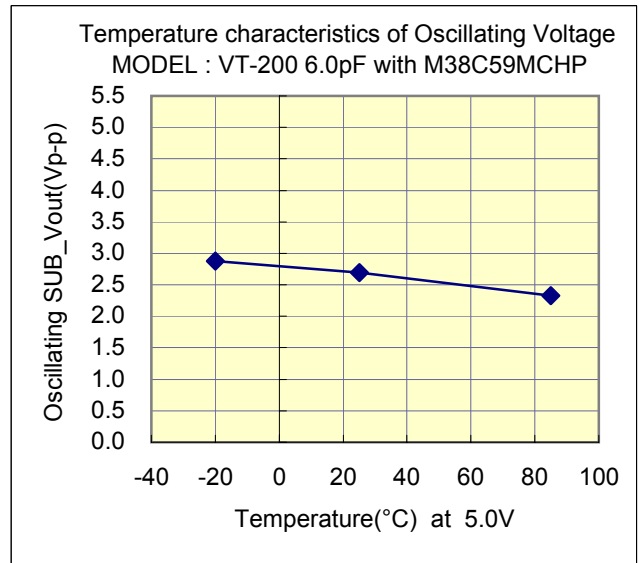
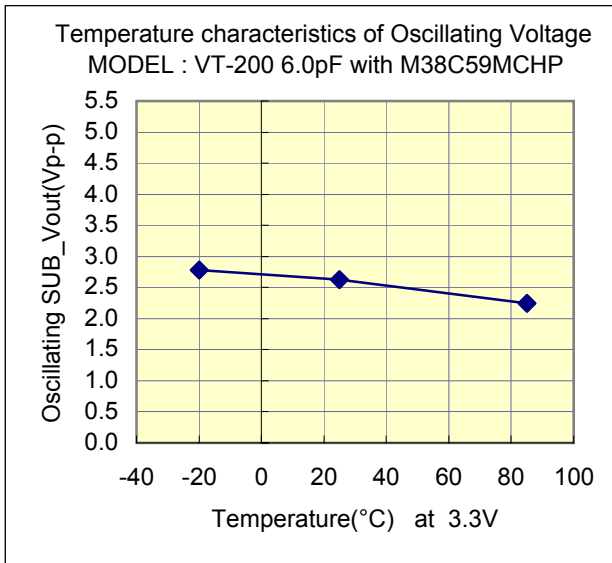


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Test Data : Temperature characteristics



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Referential components layout(see Figure 1)

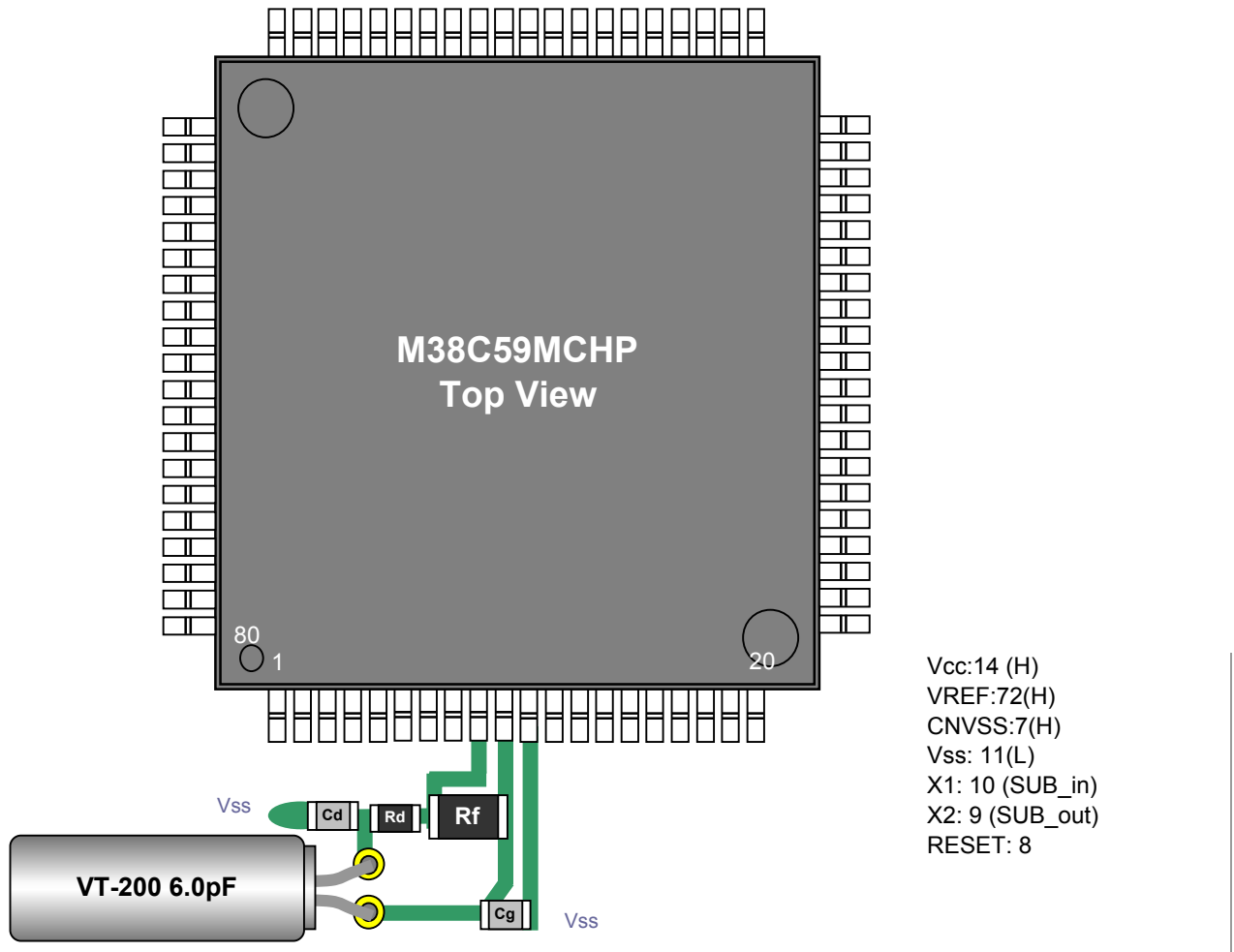


Figure 1 Referential components layout

Notes for Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

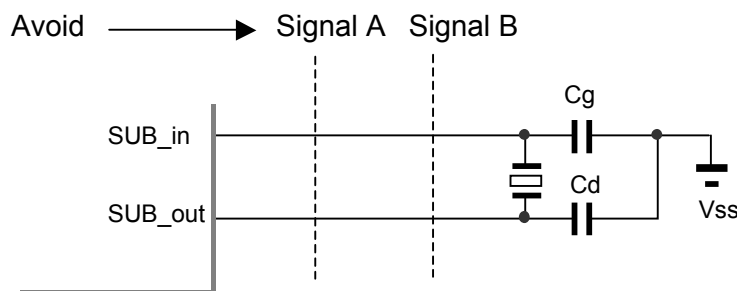


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert resistors Rd in series on the SUB_out side.

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[Evaluation Sample : VT-200 6.0pF at 25°C]

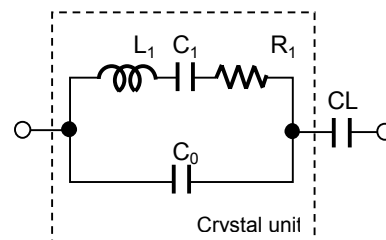
SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
VT-200 6.0pF	1	6	32768.18	32762.98	28.7	0.91	2.193	77.2
	2	6	32768.18	32763.04	27.8	0.89	2.161	80.9
	3	6	32768.19	32763.00	27.2	0.90	2.187	81.7

[IC Test Data : IC samples Rf=10M,Rd=330k ohm,Cg=4pF,Cd=5pF at 25°C]

Vcc(V)	IC samples	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart(V)	Ts(sec)
5.0	TYP	32768.259	2.40	0.01	467	1.80	0.60
	HH	32768.289	3.32	0.01	467	1.97	0.58
	HL	32768.170	-0.31	0.01	467	1.88	0.57
	LH	32768.310	3.96	0.01	467	1.77	0.59
	LL	32768.060	-3.67	0.01	467	1.96	0.52
3.3	TYP	32768.090	-2.75	0.01	507	1.80	0.56
	HH	32768.115	-1.99	0.01	507	1.97	0.62
	HL	32768.000	-5.50	0.01	507	1.88	0.57
	LH	32768.148	-0.98	0.01	507	1.77	0.62
	LL	32767.850	-10.08	0.01	467	1.96	0.50

Remark (see figure 3)

$$F_o = f_r \times \left\{ \frac{C_1}{2 \times (C_o + C_L)} + 1 \right\} \text{ (Hz)}$$



F_o : Load resonance frequency
 f_r : Resonance frequency
 R_1 : Motional resistance
 C_1 : Motional capacitance
 C_o : Shunt capacitance
 C_L : Load Capacitance

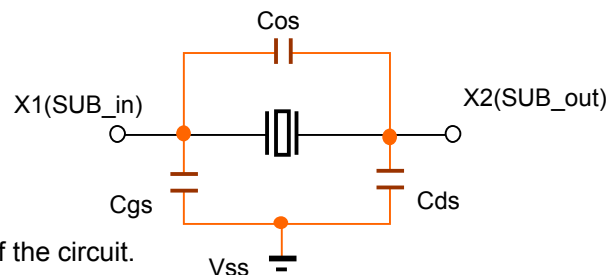
Figure 3 Equivalent circuit of crystal unit, and CL

Remark (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

$$C_L = \frac{C_g \times C_d}{C_g + C_d} + C_s \text{ (pF)}$$

Where C_s (=2 to 4pF) Stands for stray capacitance of the circuit.



C_{os} : X1_X2 Stray capacitance
 C_{gs} : X1_Vss Stray capacitance
 C_{ds} : X2_Vss Stray capacitance

Figure 4 Stray capacitance C_{os}, C_{gs}, C_{ds} of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.