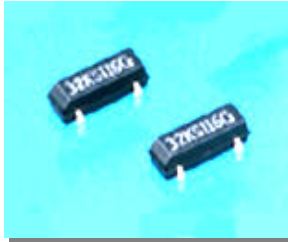
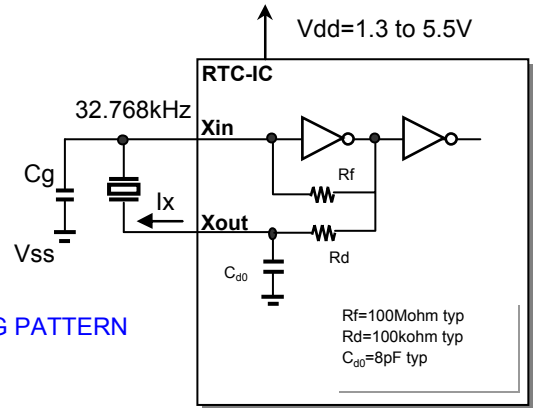


Evaluation of Subsystem Clock Oscillation Circuit

[S-78190A-16P] TSSOP(4.4x5.6) 0.65mm pitch
 Measurement conditions :3.0V, 1.3V



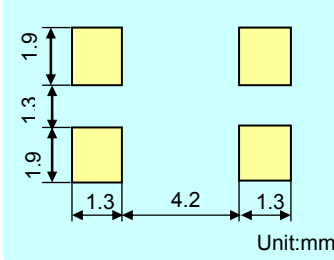
Model :SP-T2A
 Frequency :Fo=32.768kHz
 Frequency tolerance :dF/Fo= +/-20x10⁶
 Load capacitance :CL=6.0pF
 Equivalent series resistance :R1=50k ohm max
 Max. drive level :DL=1x10⁶W max
 Level of drive :DL=0.1x10⁶W typ



FEATURES

1. Plastic mold package incorporated tubular type quartz crystal.
2. Suitable for automatic and high density surface mounting.
3. Excellent shock and heat resistance
4. Real time clocks, Timers, Portable applications, Clock source for Micro-Computers

RECOMMENDED SOLDERING PATTERN



$$CL = Cg(Cd + C_{d0}) / (Cg + Cd + C_{d0}) + C_s$$

C_s: Stray capacitance

Remark) I_x : current through crystal

MODEL:SP-T2A 6.0pF with S-78190A at 25°C

Key specifications	Vdd=1.3V	Vdd=3.0V	Remarks
Negative feedback resistance : Rf (M ohm)	Built-in	Built-in	
Current control resistance : Rd (k ohm)	Built-in	Built-in	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	5	5	Optimal capacitance in response to CL
Capacitance at drain : Cd (pF)	Built-in	Built-in	(CL = (Cd+C _{d0}) // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vdd=1.3V	Vdd=3.0V	Remarks
Matching Accuracy : df / f (x10 ⁻⁶)	-0.1	-0.1	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V (x10 ⁻⁶)	0.0	0.0	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL (x10 ⁻⁶ W)	0.01	0.01	DL=I _x ² Re < 1x10 ⁻⁶ W, Re=R1(1 + Co / CL) ²
Negative resistance : - RL (kohm)	554	554	5 times larger than R _{1MAX}
Oscillation allowance : M (times)	11.1	11.1	Judgemental standard of oscillation stability
Voltage of oscillation start : Vstart (V)	0.90	0.90	
Voltage of oscillation stop : Vstop (V)	0.64	0.64	
Oscillation start up time : Ts (sec)	0.28	0.14	Time to reach 90% of output level

Temperature characteristics of circuit		Vdd=1.3V	Vdd=3.0V	Remarks
at -40°C	Variation : df / T (x10 ⁻⁶)	-138	-138	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)
at +85°C	Variation : df / T (x10 ⁻⁶)	-130	-130	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

Seiko Instruments USA Inc.

2990, West Lomita Blvd., Torrance, CA 90505, U.S.A
 Telephone : +1 310-517-7771 Facsimile : +1 310-517-7792
 Email : crystals@siu-la.com

Seiko Instruments GmbH

Siemensstrasse 9, D-63263 Neu-Isenburg, Germany
 Telephone : +49-6102-297-0 Facsimile : +49-6102-297-320
 Email : info@seiko-instruments.de

Seiko Instruments Inc.

1-8, Nakase, Mihama-ku, Chiba-shi, Chiba 261-8507, Japan
 Facsimile : +81-43-211-8030
 E-mail : component@sii.co.jp



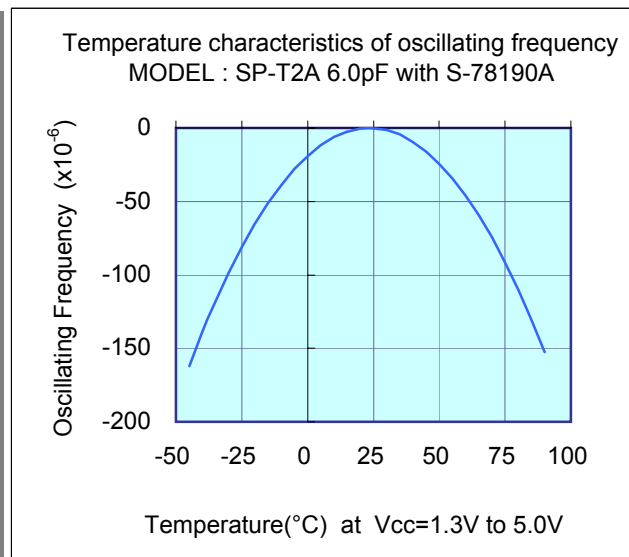
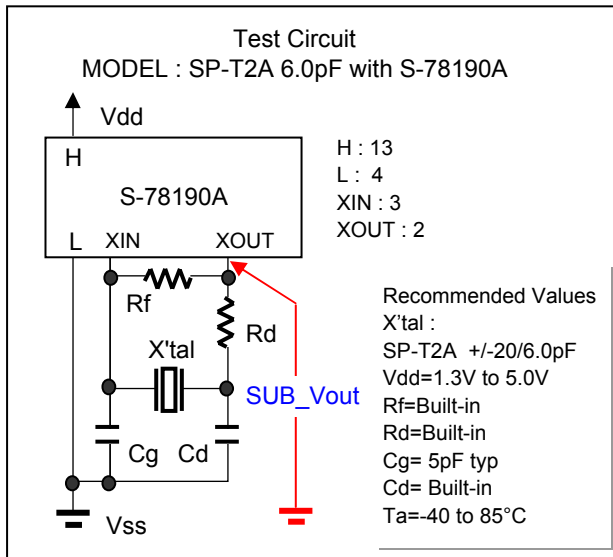
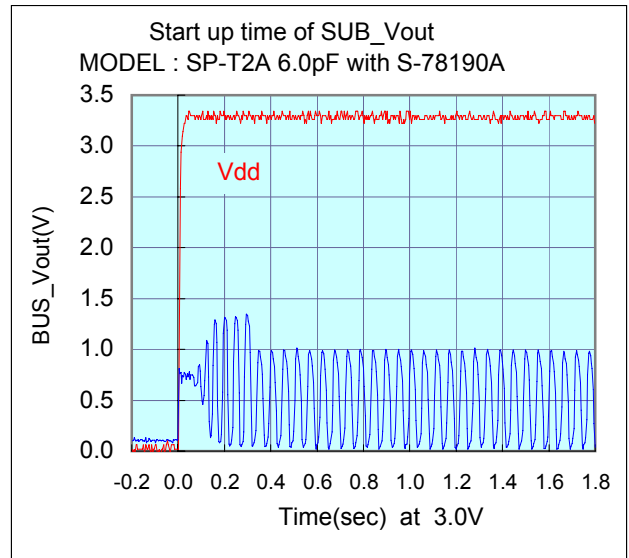
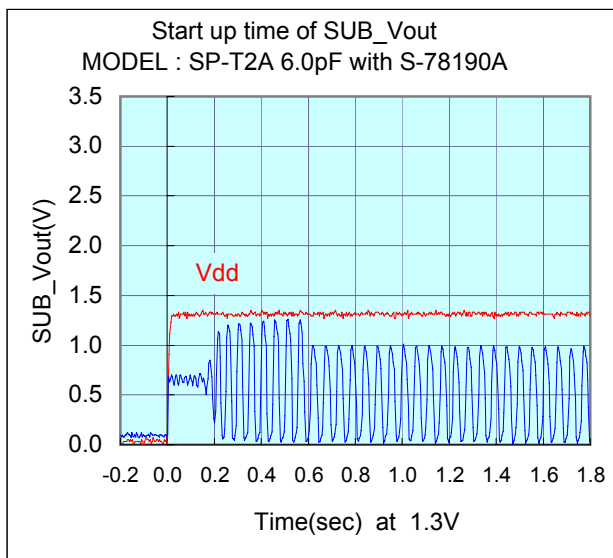
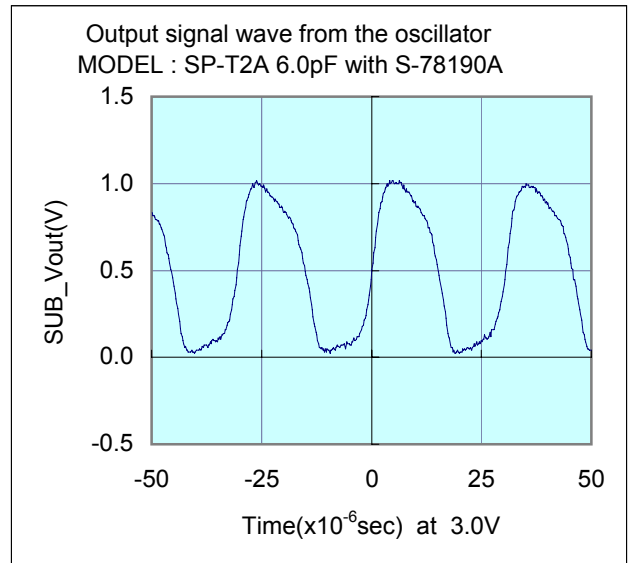
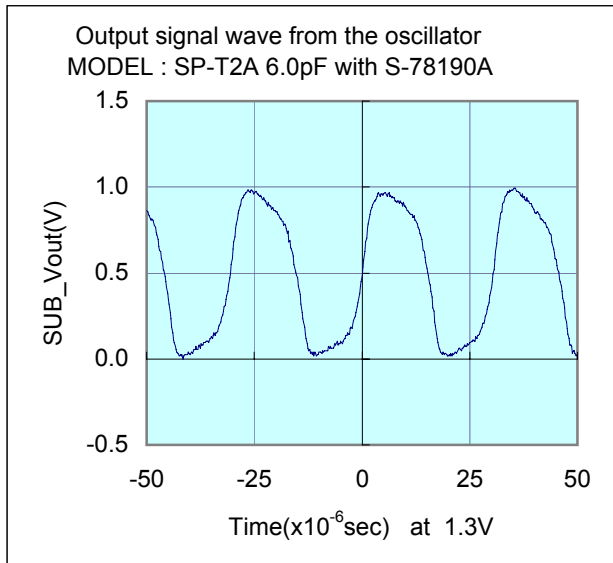
Seiko Instruments Inc.
 Phone: +81-43-211-1207(Direct)

Evaluation of Subsystem Clock Oscillation Circuit

[S-78190A-16P] TSSOP(4.4x5.6) 0.65mm pitch
 Measurement conditions :3.0V, 1.3V



Test Data at 25°C

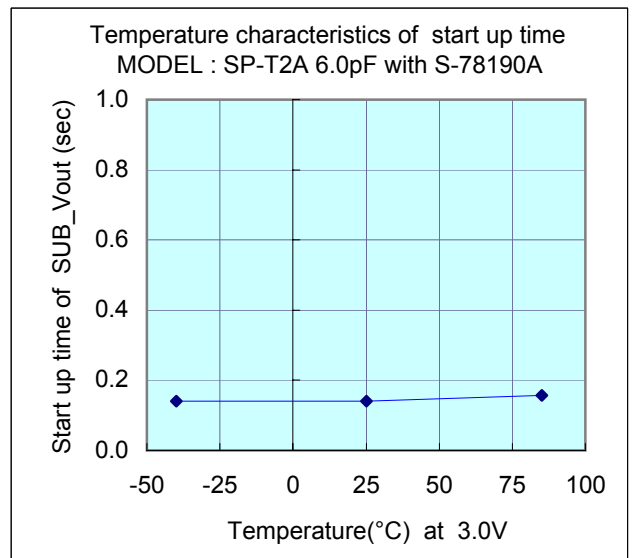
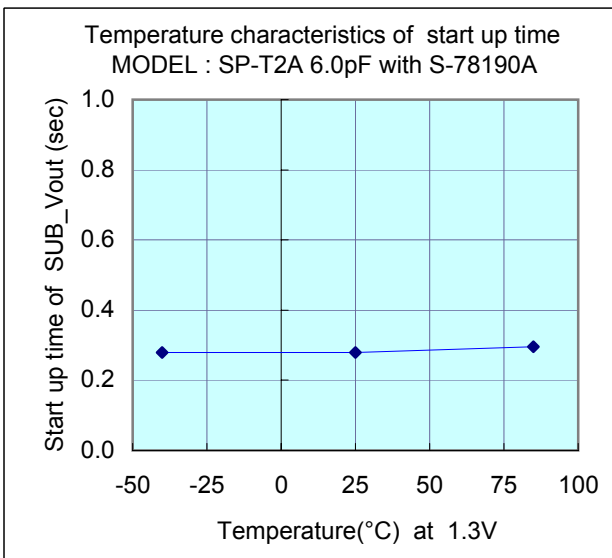
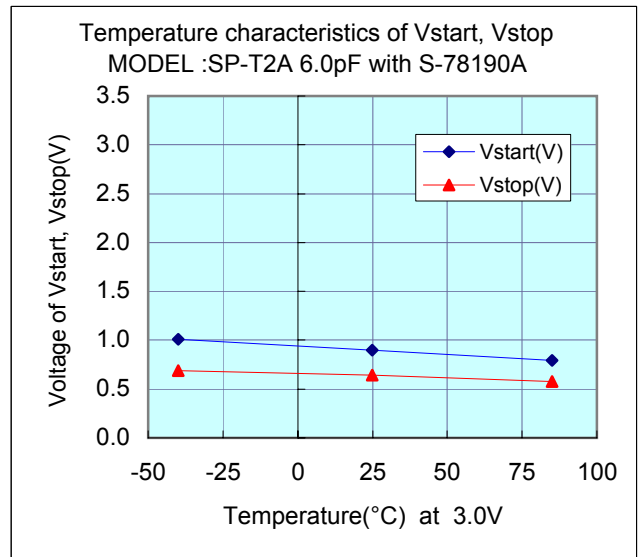
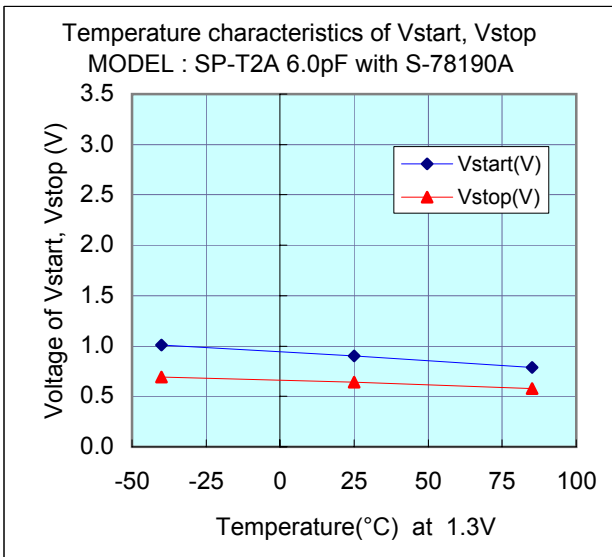
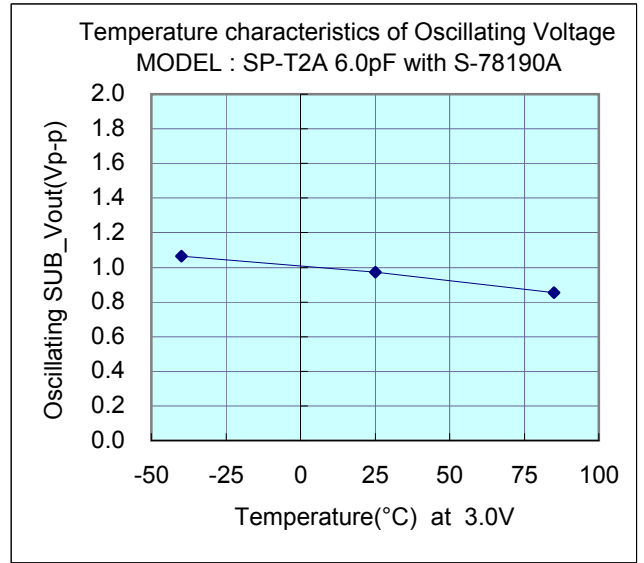
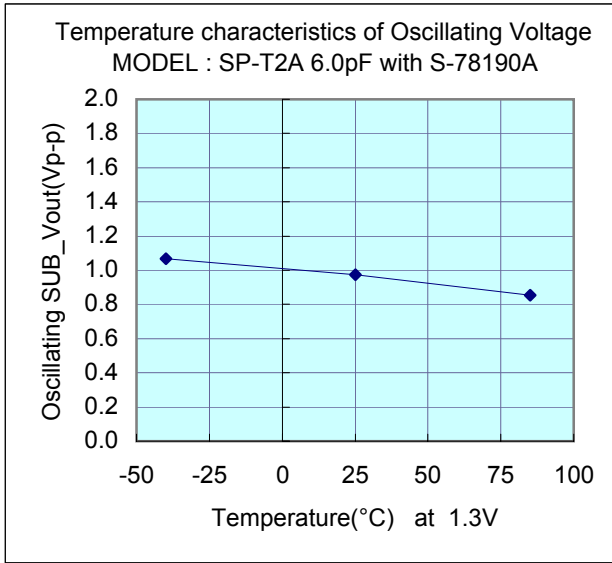


Evaluation of Subsystem Clock Oscillation Circuit

[S-78190A-16P] TSSOP(4.4x5.6) 0.65mm pitch
 Measurement conditions :3.0V, 1.3V



Test Data : Temperature characteristics



Evaluation of Subsystem Clock Oscillation Circuit

[S-78190A-16P] TSSOP(4.4x5.6) 0.65mm pitch
 Measurement conditions :3.0V, 1.3V



Referential components layout(see Figure 1)

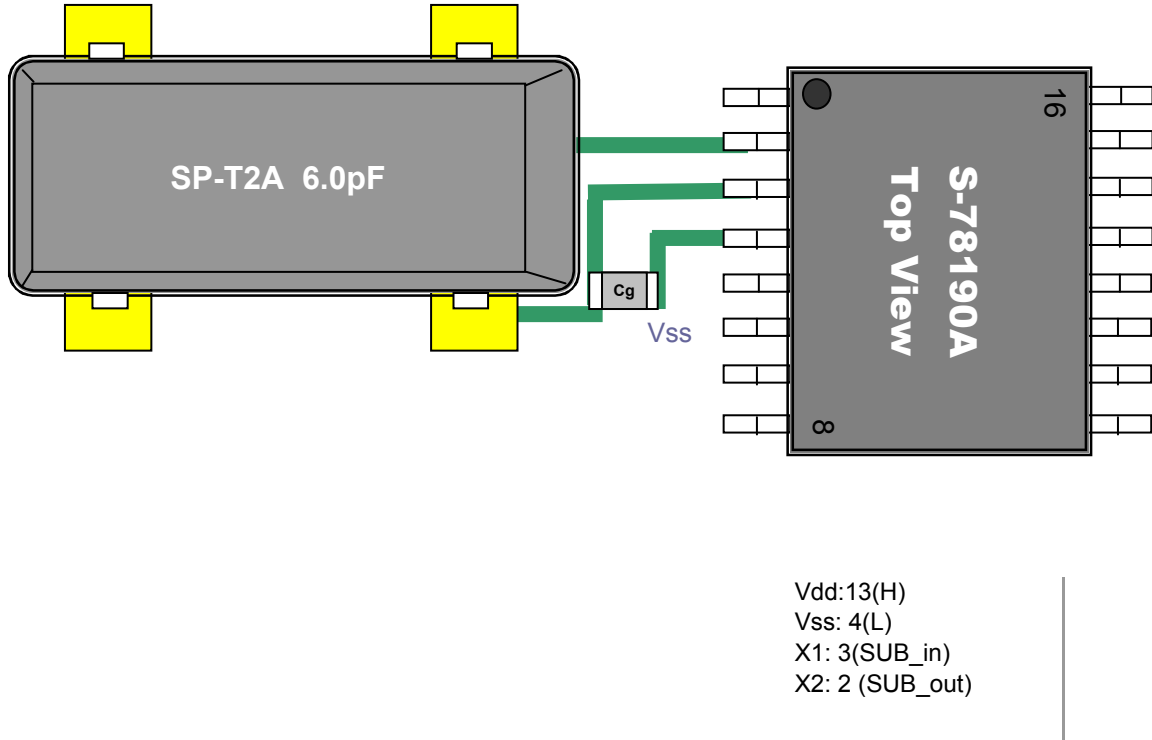


Figure 1 Referential components layout

Notes for Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.
 Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

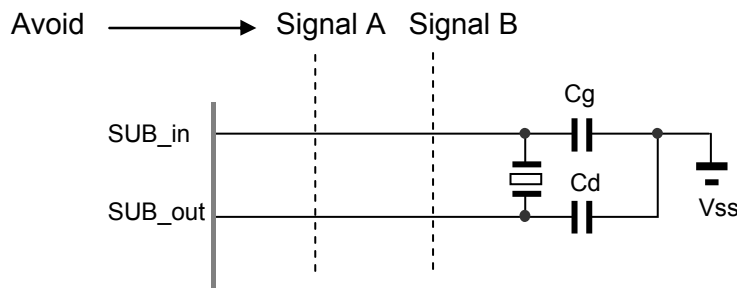


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert resistors Rd in series on the SUB_out side.

Evaluation of Subsystem Clock Oscillation Circuit

[S-78190A-16P] TSSOP(4.4x5.6) 0.65mm pitch
 Measurement conditions :3.0V, 1.3V



[Evaluation Sample : SP-T2A 6.0pF at 25°C]

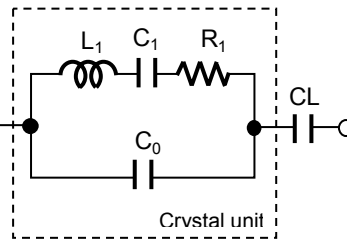
SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
SP-T2A 6.0pF	1	6	32768.34	32763.01	31.6	0.94	2.258	68.1
	2	6	32768.20	32762.87	32.4	0.93	2.255	66.5
	3	6	32768.28	32762.95	31.5	0.93	2.255	68.4

[IC Test Data : IC sample Rf=Built-in,Rd=Built-in,Cg=5pF,Cd=Built-in at 25°C]

Vdd(V)	IC samples	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart(V)	Ts(sec)
3.0	TYP	32768.197	-0.09	0.01	554	0.90	0.14
	HH	32768.270	2.14	0.01	554	1.04	0.13
	HL	32768.180	-0.61	0.01	604	0.86	0.18
	LH	32768.250	1.53	0.02	514	0.88	0.20
	LL	32768.160	-1.22	0.01	604	0.90	0.17
1.3	TYP	32768.197	-0.09	0.01	554	0.90	0.28
	HH	32768.270	2.14	0.01	554	1.04	0.30
	HL	32768.180	-0.61	0.01	604	0.86	0.23
	LH	32768.250	1.53	0.02	514	0.88	0.29
	LL	32768.160	-1.22	0.01	604	0.90	0.22

Remark (see figure 3)

$$Fo = fr \times \{ C1 / (2 \times (Co + CL)) + 1 \} \text{ (Hz)}$$



- Fo : Load resonance frequency
- fr : Resonance frequency
- R1 : Motional resistance
- C1 : Motional capacitance
- Co : Shunt capacitance
- CL : Load Capacitance

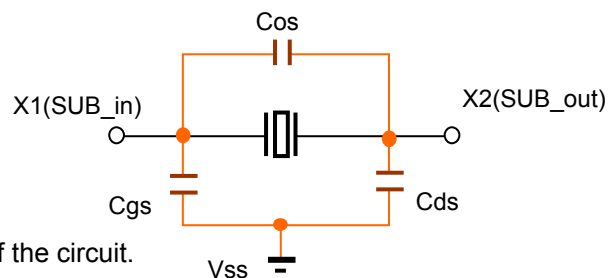
Figure 3 Equivalent circuit of crystal unit, and CL

Remark (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

$$CL = Cg \times Cd / (Cg + Cd) + Cs \text{ (pF)}$$

Where Cs(=2 to 4pF) Stands for stray capacitance of the circuit.



- Cos : X1_X2 Stray capacitance
- Cgs : X1_Vss Stray capacitance
- Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.