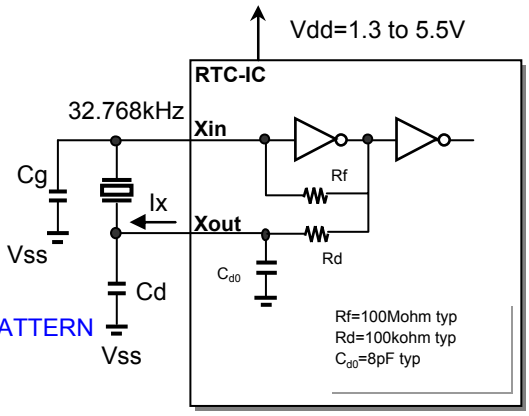
Evaluation of Subsystem Clock Oscillation Circuit

[S-78190A-16P] TSSOP(4.4x5.6) 0.65mm pitch
Measurement conditions :3.0V, 1.3V

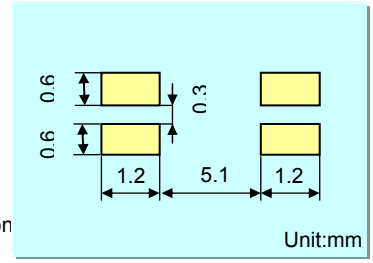
Model	:SSP-T7
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10^{6}
Load capacitance	:CL=7.0pF
Equivalent series resistance	:R1=65kohm max
Max. drive level	:DL=1x10^{-6}W max
Level of drive	:DL=0.1x10^{-6}W typ



FEATURES

1.Ultra thin type with 1.4mm Max.
2.SMD type suitable for automatic & high density surface mounting.
3.Plastic mold package containing highly reliable tubular type quartz crystal.
4.Excellent shock and heat resistance.
5.Cellular phones,PDA,Radio communication equipment, Portable applications etc.

RECOMMENDED SOLDERING PATTERN



$CL=Cg(Cd+C_{d0})/(Cg+Cd+C_{d0})+C_s$
C_s ;Stray capacitance

Remark) Ix : current through crystal

MODEL:SSP-T7 7.0pF with S-78190A at 25°C

Key specifications	Vdd=1.3V	Vdd=3.0V	Remarks
Negative feedback resistance : Rf (M ohm)	Bulit-in	Bulit-in	
Current control resistance : Rd (k ohm)	Bulit-in	Bulit-in	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	9	9	Optimal capacitance in response to CL
Capacitance at drain : Cd (pF)	2	2	(CL = (Cd+C_{d0}) // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vdd=1.3V	Vdd=3.0V	Remarks
Matching Accuracy : df / f (x10^{-6})	1.1	1.1	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V (x10^{-6})	0.0	0.0	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL (x10^{-6}W)	0.02	0.02	DL=Ix^2 Re < 1x10^{-6}W,Re=R1(1 + Co / CL)^2
Negative resistance : | - RL | (kohm)	378	378	5 times larger than R_{1MAX}
Oscillation allowance : M (times)	5.8	5.8	Judgemental standard of oscillation stability
Voltage of oscillation start : Vstart (V)	0.62	0.62	
Voltage of oscillation stop : Vstop (V)	0.55	0.55	
Oscillation start up time : Ts (sec)	0.16	0.15	Time to reach 90% of output level

Temperature characteristics of circuit		Vdd=1.3V	Vdd=3.0V	Remarks
at -40°C	Variation : df / T (x10^{-6})	-135	-135	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^2)
at +85°C	Variation : df / T (x10^{-6})	-128	-128	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^2)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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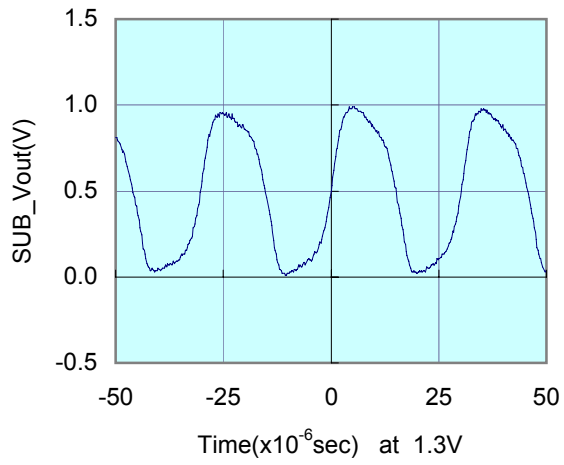
Measurement conditions :3.0V, 1.3V

Test Data at 25°C

Output signal wave from the oscillator
MODEL : SSP-T7 7.0pF with S-78190A



Output signal wave from the oscillator
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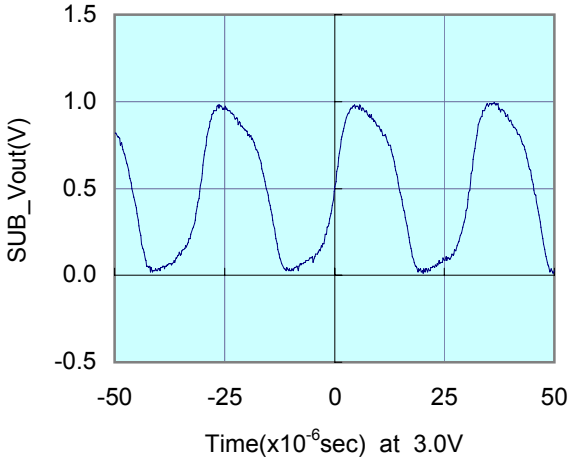
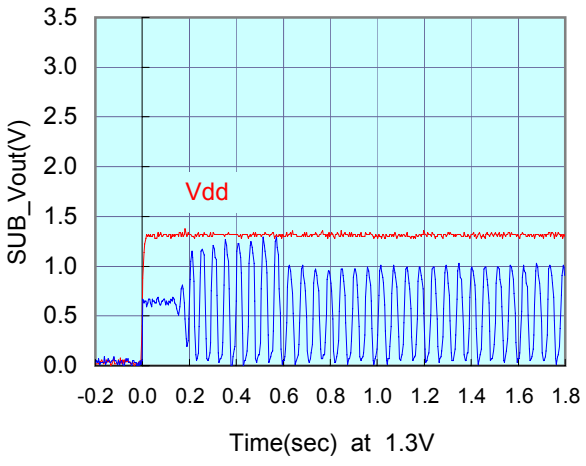
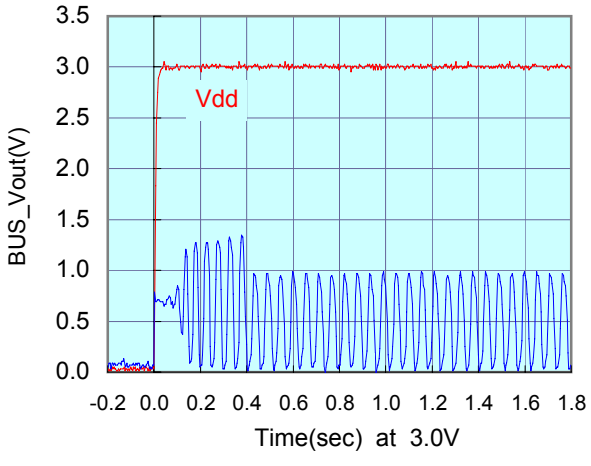


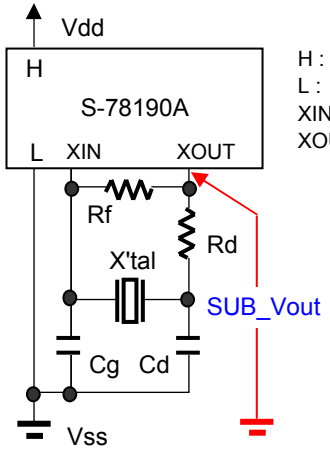
Start up time of SUB_Vout
MODEL : SSP-T7 7.0pF with S-78190A



Start up time of SUB_Vout
MODEL : SSP-T7 7.0pF with S-78190A



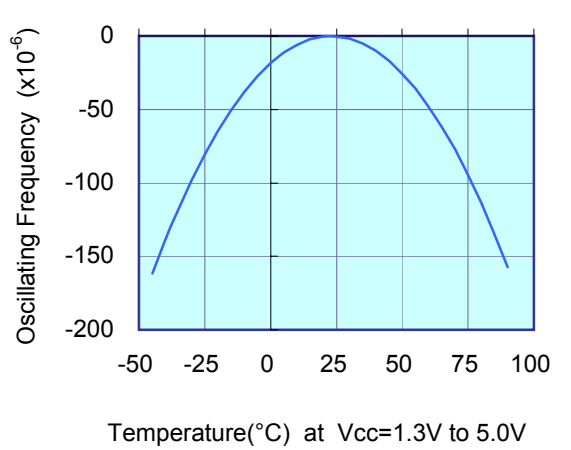
Test Circuit
MODEL : SSP-T7 7.0pF with S-78190A



H : 13
L : 4
XIN : 3
XOUT : 2

Recommended Values
X'tal :
SSP-T7 +/-20/7.0pF
Vdd=1.3V to 5.0V
Rf=Built-in
Rd=Built-in
Cg= 9pF typ
Cd= 2pF typ
Ta=-40 to 85°C

Temperature characteristics of oscillating frequency
MODEL : SSP-T7 7.0pF with S-78190A



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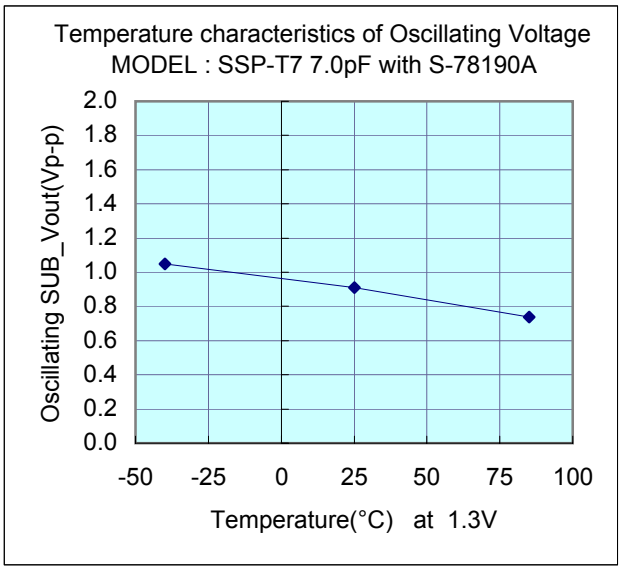
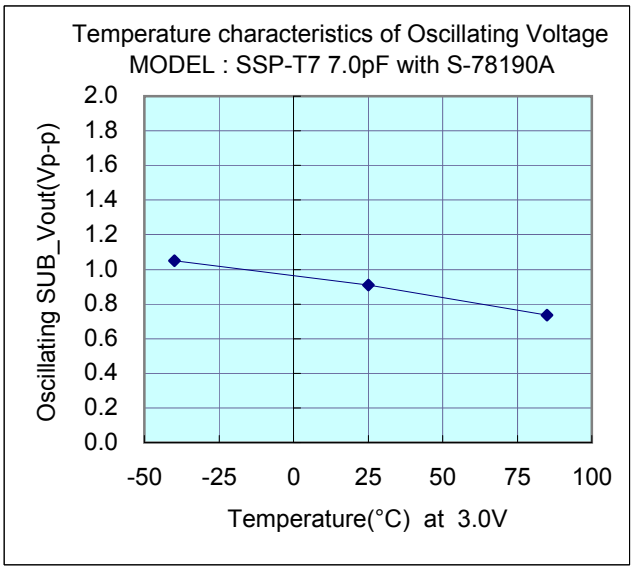
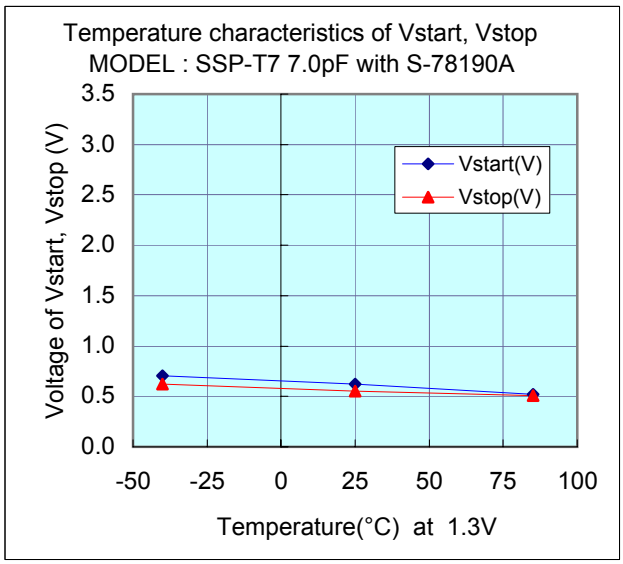
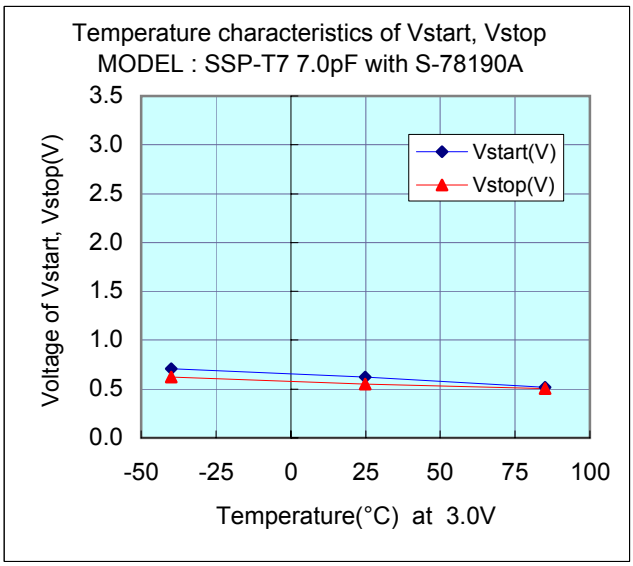
[S-78190A-16P] TSSOP(4.4x5.6) 0.65mm pitch
Measurement conditions :3.0V, 1.3V

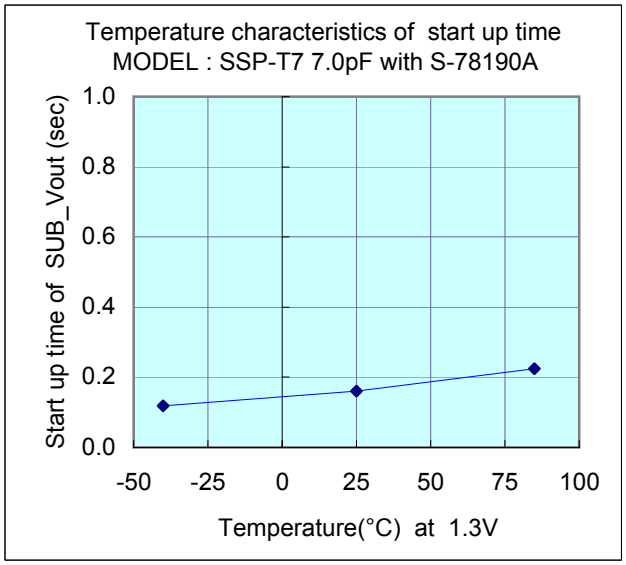
Test Data : Temperature characteristics

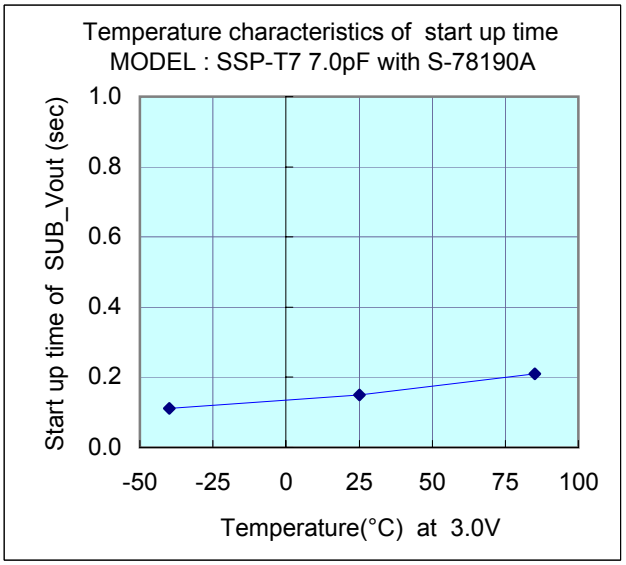












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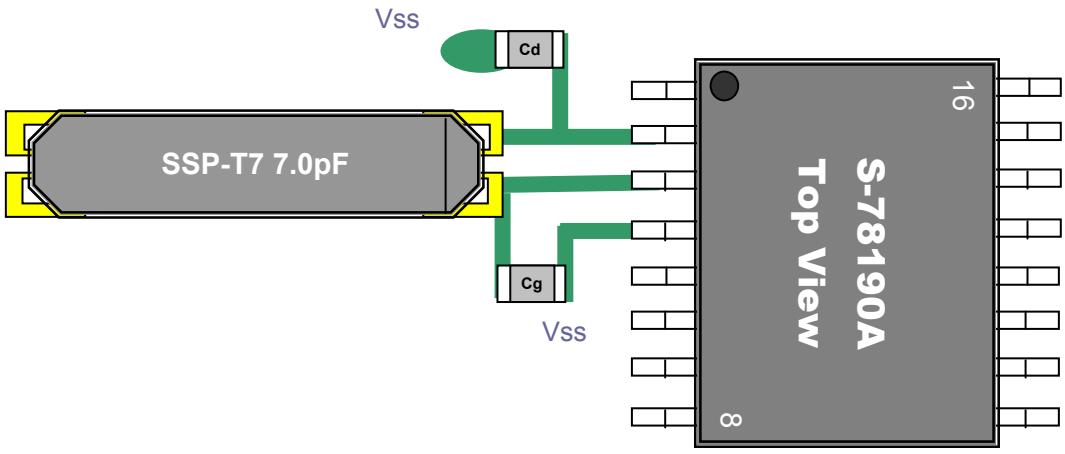
Evaluation of Subsystem Clock Oscillation Circuit

[S-78190A-16P] TSSOP(4.4x5.6) 0.65mm pitch
Measurement conditions :3.0V, 1.3V

Referential components layout(see Figure 1)



Vdd:13(H)
Vss: 4(L)
X1: 3(SUB_in)
X2: 2 (SUB_out)

Figure 1 Referential components layout

Notes for Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.
Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

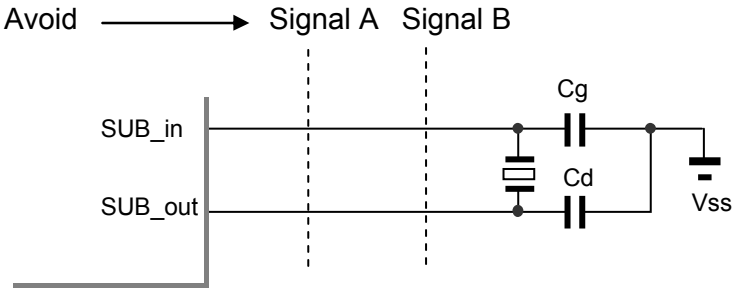


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert resistors Rd in series on the SUB_out side.

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[S-78190A-16P] TSSOP(4.4x5.6) 0.65mm pitch
Measurement conditions :3.0V, 1.3V

[Evaluation Sample : SSP-T7 7.0pF at 25°C]

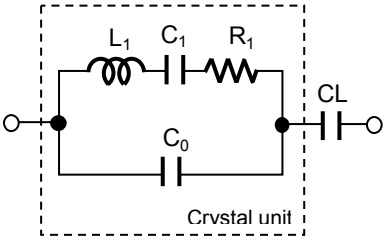
SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
SSP-T7 7.0pF	1	7	32767.91	32763.77	37.9	0.86	1.985	64.6
	2	7	32767.88	32763.63	39.2	0.85	2.037	60.9
	3	7	32767.83	32763.68	40.3	0.83	1.983	60.8

[IC Test Data : IC sample Rf=Built-in,Rd=Built-in,Cg=9pF,Cd=2pF at 25°C]

Vdd(V)	IC samples	Fosc(Hz)	df / f(x10^{-6})	DL(x10^{-6}W)	| -RL |(kohm)	Vstart(V)	Ts(sec)
3.0	TYP	32767.945	1.07	0.02	378	0.62	0.15
	HH	32768.030	3.66	0.02	378	0.70	0.12
	HL	32767.940	0.92	0.01	408	0.83	0.22
	LH	32768.010	3.05	0.02	348	0.89	0.19
	LL	32767.918	0.24	0.01	408	0.70	0.15
1.3	TYP	32767.945	1.07	0.02	378	0.62	0.16
	HH	32768.030	3.66	0.02	378	0.70	0.50
	HL	32767.940	0.92	0.01	408	0.83	0.24
	LH	32768.010	3.05	0.02	348	0.89	0.34
	LL	32767.918	0.24	0.01	408	0.70	0.17

Remark (see figure 3)

$$Fo = fr \times \{ C1/ (2\times(Co + CL)) + 1 \} \quad (Hz)$$



Fo : Load resonance frequency
fr : Resonance frequency
R1 : Motional resistance
C1 : Motional capacitance
Co : Shunt capacitance
CL : Load Capacitance

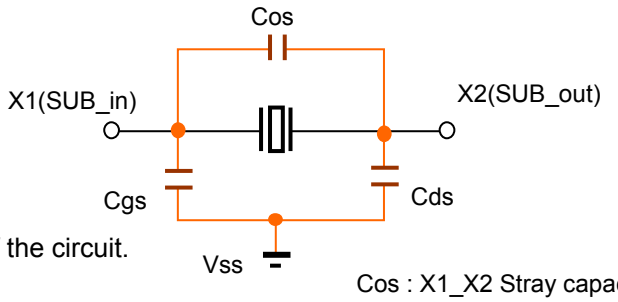
Figure 3 Equivalent circuit of crystal unit, and CL

Remark (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

$$CL = Cg\times Cd / (Cg + Cd) + Cs \quad (pF)$$

Where Cs(=2 to 4pF) Stands for stray capacitance of the circuit.



Cos : X1_X2 Stray capacitance
Cgs : X1_Vss Stray capacitance
Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

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