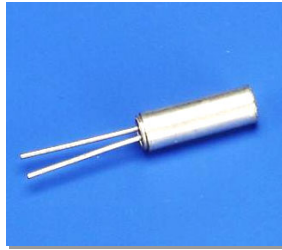


Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1168GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V

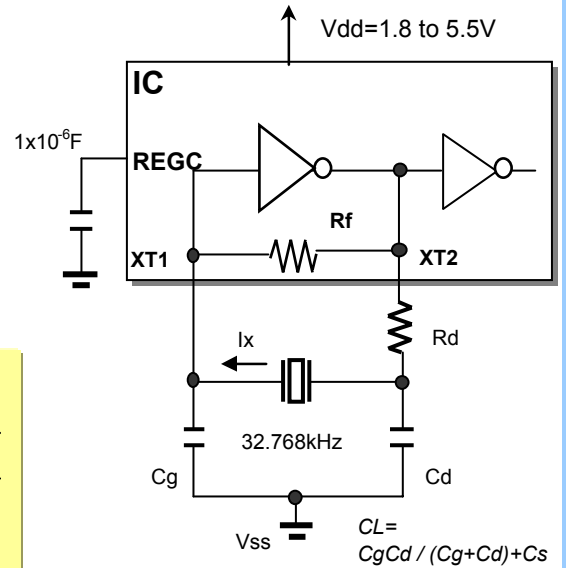
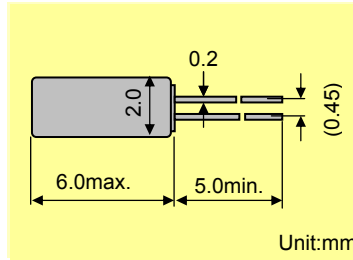


Model	:VT-200
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10 ⁶
Load capacitance	:CL=6.0pF
Equivalent series resistanc	:R1=50kohm max
Max. drive level	:DL=x10 ⁻⁶ W max
Level of drive	:DL=0.1x10 ⁻⁶ W typ

FEATURES

- 1.Compact tubular package
- 2.Photolithographic process
- 3.Excellent shock resistance and environmental characteristics.
- 4.Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)



Remark) I_x : current through crystal

MODEL:VT-200 6.0pF with uPD78F1168GC at 25°C

Key specifications	Low(*1)	Normal(*2)	Remarks
Current control resistance : Rd (k ohm)	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	(5)	(5)	Optimal capacitance in response to CL
Capacitance at drain : Cd (pF)	(5)	(5)	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Low(*1)	Normal(*2)	Remarks
Matching Accuracy : df / f (x10 ⁻⁶)	1.4	10.5	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V (x10 ⁻⁶)	0.0	0.0	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL (x10 ⁻⁶ W)	0.01	0.01	DL=Ix ² Re < 1x10 ⁻⁶ W, Re=R1(1 + Co / CL) ²
Negative resistance : - RL (kohm)	427	467	5 times larger than R _{1MAX}
Oscillation allowance : M (times)	8.5	9.3	Judgemental standard of oscillation stability
Voltage of oscillation start : Vstart (V)	1.60	1.60	
Voltage of oscillation stop : Vstop (V)	1.59	1.59	
Oscillation start up time : Ts (sec)	1.28	1.28	Time to reach 90% of output level

Temperature characteristics of circuit		Low(*1)	Normal(*2)	Remarks
at -40°C	Variation : df / T (x10 ⁻⁶)	-139	-139	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)
at +85°C	Variation : df / T (x10 ⁻⁶)	-127	-127	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

*1; low consumption current mode

*2; normal current mode

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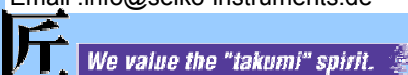
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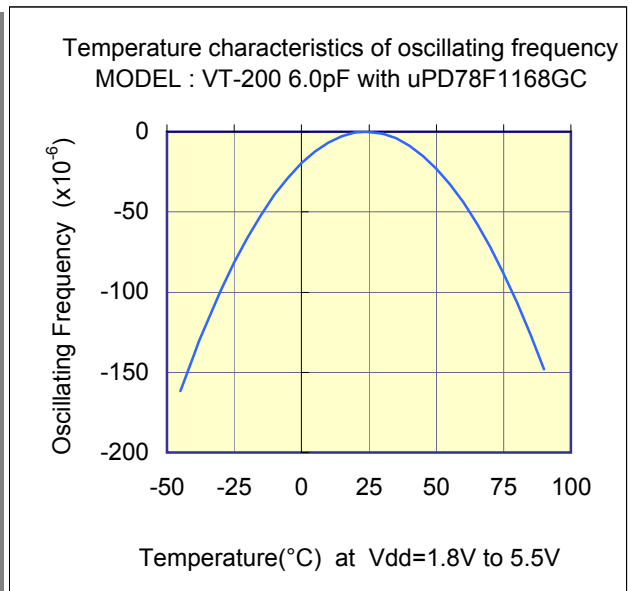
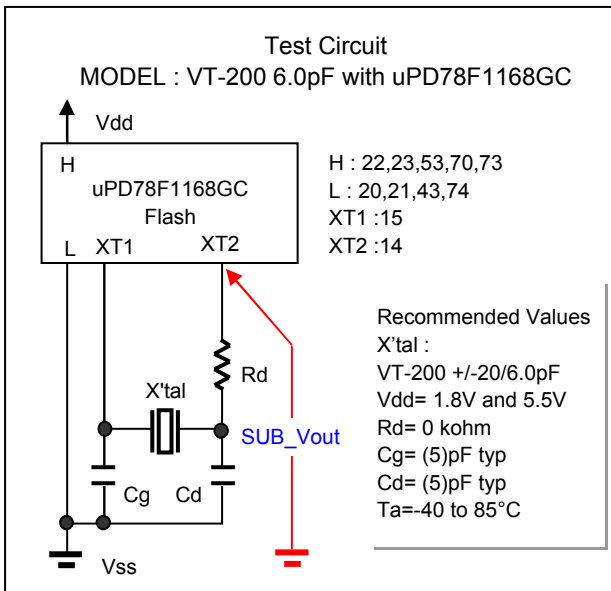
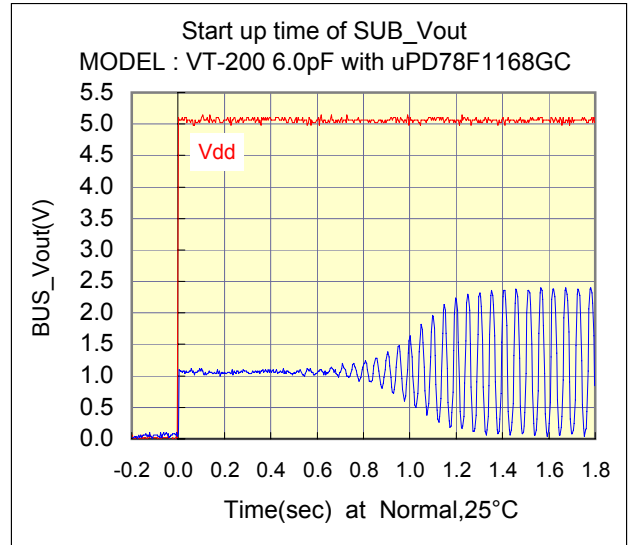
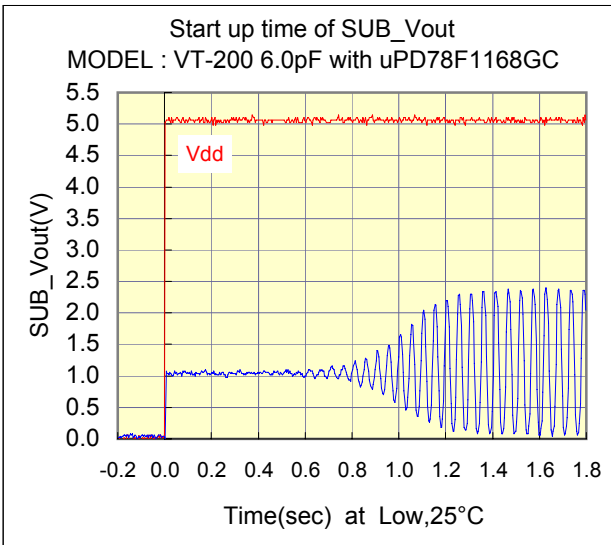
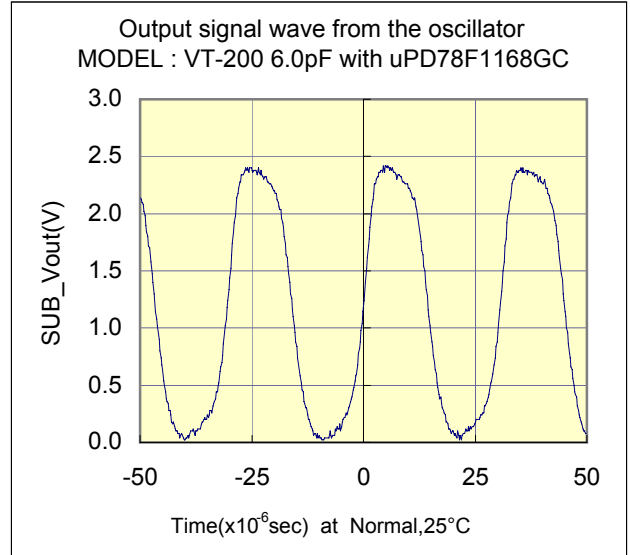
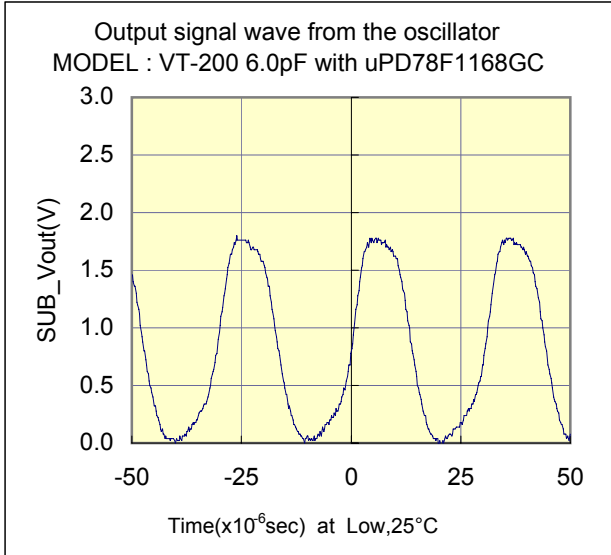
Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1168GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



Test Data



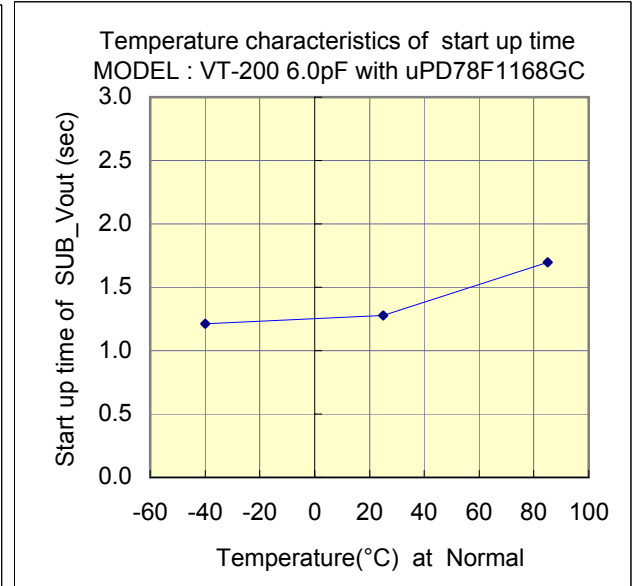
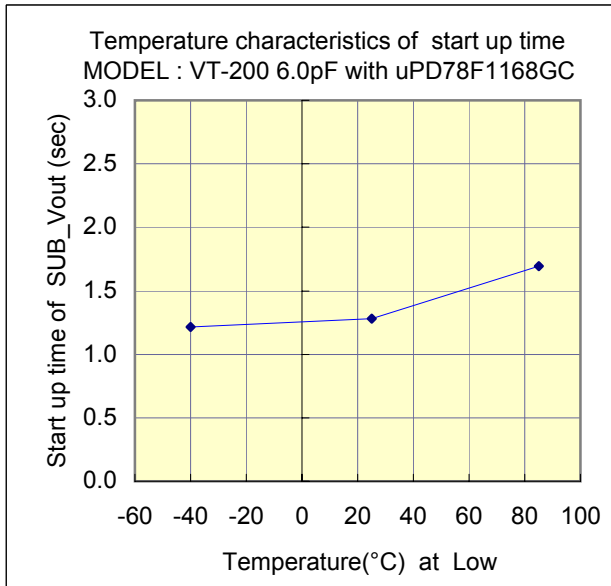
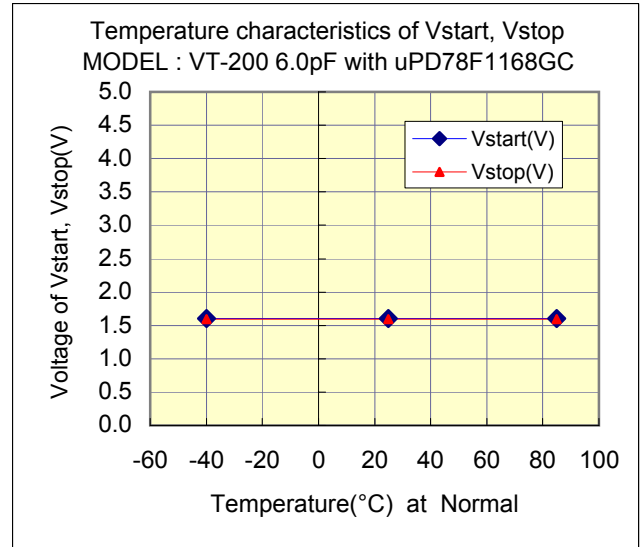
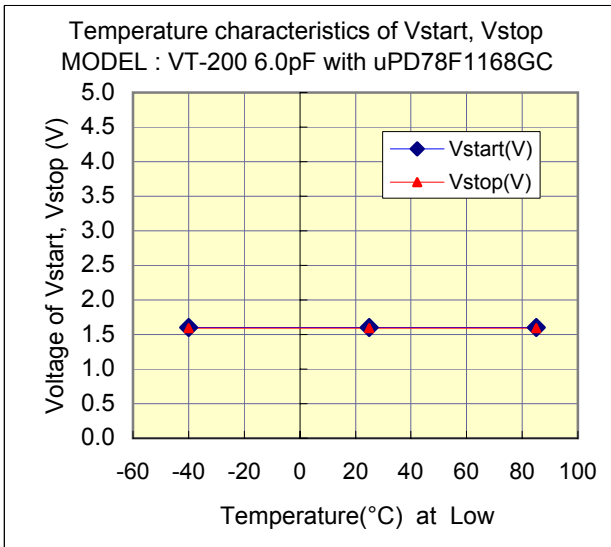
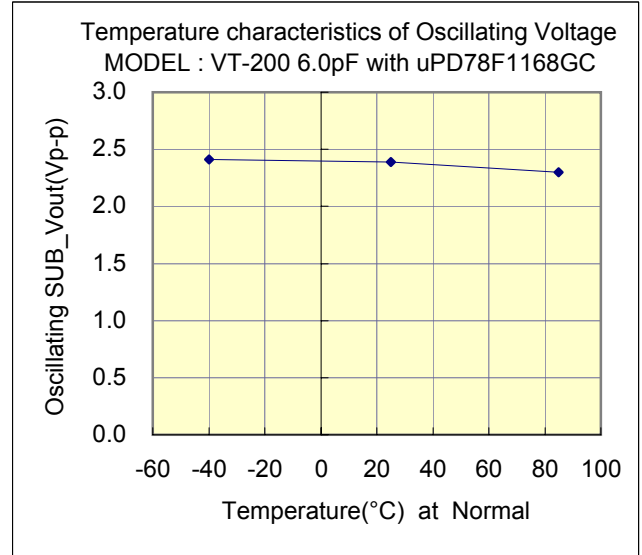
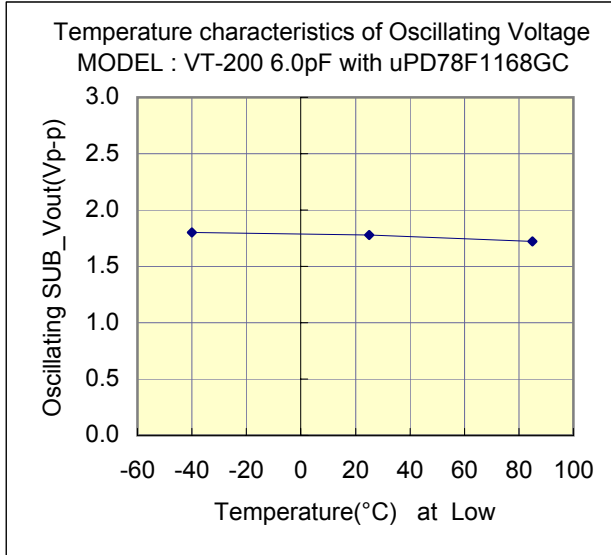
Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1168GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



Test Data : Temperature characteristics



Evaluation of Subsystem Clock Oscillation Circuit

[μ PD78F1168GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



Referential components layout(see Figure 1)

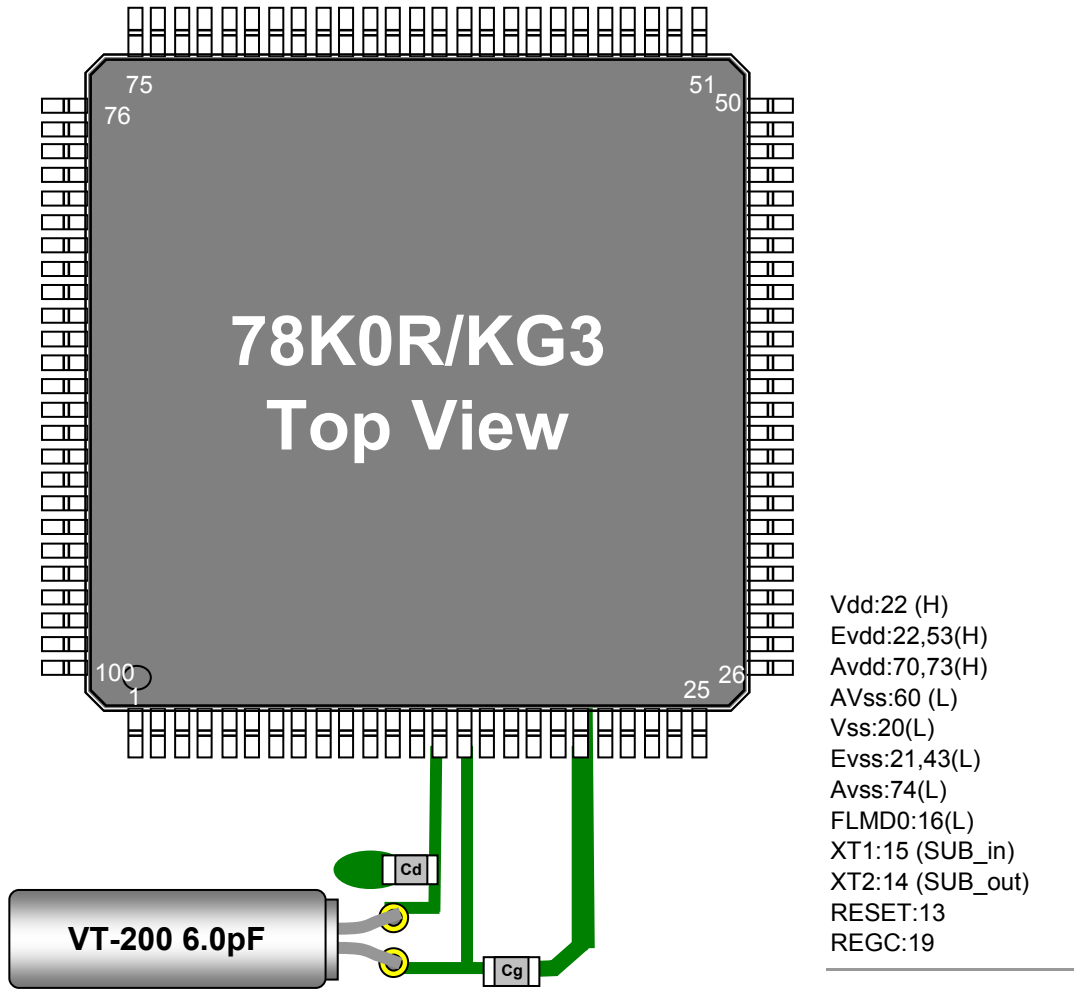


Figure 1 Referential components layout

Notes for Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

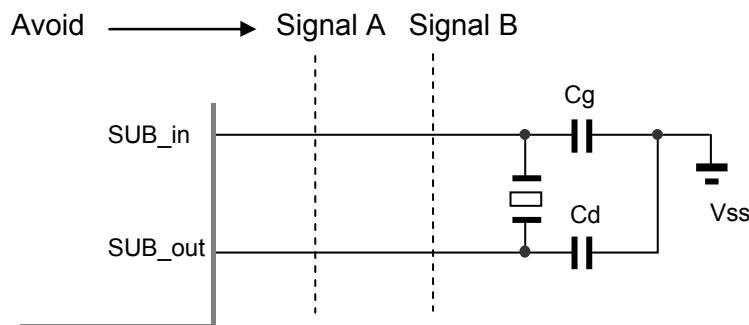


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert resistors R_d in series on the SUB_out side.

Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1168GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



[Evaluation Sample : VT-200 6.0pF at 25°C]

SAMPLE	No.	CL (pF)	Fo(Hz)	fr (Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
VT-200 6.0pF	1	6	32768.18	32762.98	28.7	0.91	2.193	77.2
	2	6	32768.18	32763.04	27.8	0.89	2.161	80.9
	3	6	32768.01	32762.79	28.0	0.90	2.199	78.9

[IC Test Data : IC Sample Rd=0 kohm,Cg=5pF,Cd=5pF at 25°C]

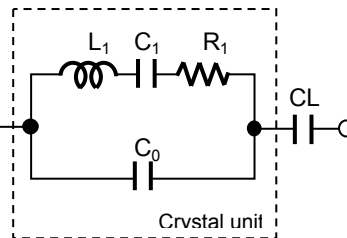
Power mode	IC Sample	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart(V)	Ts(sec)
Normal	TYP	32768.36	10.53	0.01	467	1.60	1.28
	HH	32768.30	8.85	0.01	467	1.60	1.27
	HL	32768.47	14.04	0.01	467	1.60	1.27
	LH	32768.29	8.45	0.01	467	1.61	1.29
	LL	32768.43	12.66	0.01	467	1.60	1.32

[IC Test Data : IC Sample Rd=0 kohm,Cg=5pF,Cd=5pF at 25°C]

Power mode	IC Sample	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart(V)	Ts(sec)
Low	TYP	32768.06	1.40	0.01	427	1.60	1.28
	HH	32767.98	-0.79	0.01	397	1.60	1.27
	HL	32768.08	2.14	0.01	427	1.60	1.27
	LH	32767.98	-0.92	0.01	397	1.61	1.29
	LL	32768.10	2.75	0.01	427	1.60	1.32

Remark (see figure 3)

$$Fo = fr \times \left\{ \frac{C1}{2 \times (Co + CL)} + 1 \right\} \text{ (Hz)}$$



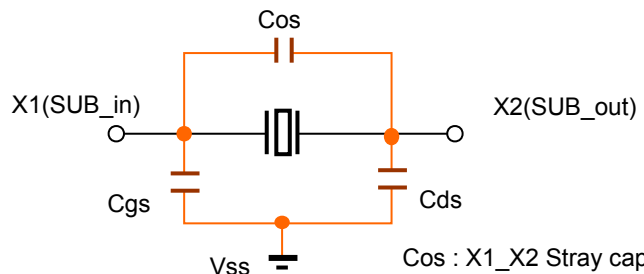
Fo : Load resonance frequency
fr : Resonance frequency
R1 : Motional resistance
C1 : Motional capacitance
Co : Shunt capacitance
CL : Load Capacitance

Figure 3 Equivalent circuit of crystal unit, and CL

Remark (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

$$CL = Cg \times Cd / (Cg + Cd) + Cs \text{ (pF)}$$



Cos : X1_X2 Stray capacitance
Cgs : X1_Vss Stray capacitance
Cds : X2_Vss Stray capacitance

Where Cs(=2 to 4pF) Stands for stray capacitance of the circuit.

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.



Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1168GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : Vdd=(1.6V) to (6.0V) at 25°C

Referential Data : Voltage characteristics

