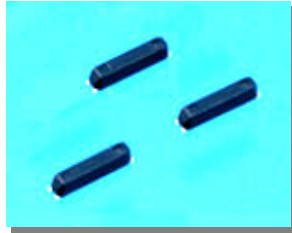


# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1168GC-16BT] LQFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V

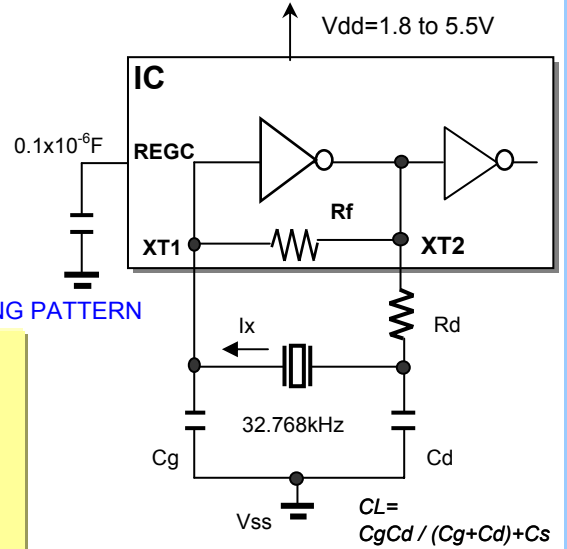
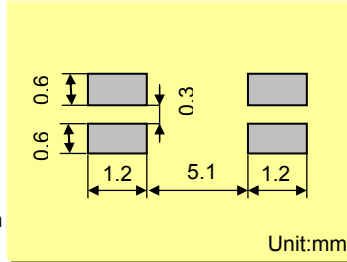


Model	:SSP-T7
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10 <sup>-6</sup>
Load capacitance	:CL= 7.0pF
Equivalent series resistance	:R1=65kohm max
Max. drive level	:DL=1x10 <sup>-6</sup> W max
Level of drive	:DL=0.1x10 <sup>-6</sup> W typ

## FEATURES

- 1.Ultra thin type with 1.4mm Max.
- 2.SMD type suitable for automatic & high density surface mounting.
- 3.Plastic mold package containing highly reliable tubular type quartz crystal.
- 4.Excellent shock and heat resistance.
- 5.Cellular phones,PDA,Radio communication equipment, Portable applications etc.

## RECOMMENDED SOLDERING PATTERN



MODEL:SSP-T7 7.0pF with uPD78F1168GC at 25°C

Key specifications	Low(*1)	Normal(*2)	Remarks
Current control resistance : Rd ( k ohm )	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg ( pF )	(7)	(7)	Optimal capacitance in response to CL ( CL = Cd // Cg + stray capacitance )
Capacitance at drain : Cd ( pF )	(7)	(7)	

Circuit characteristics ( at 25°C )	Low(*1)	Normal(*2)	Remarks
Matching Accuracy : $df / f$ ( $\times 10^{-6}$ )	0.3	6.4	Frequency offset volume at specified Vdd
Voltage Fluctuation : $\pm df / V$ ( $\times 10^{-6}$ )	0.0	0.0	Vdd +/-10% ( Standard operating voltage range )
Drive Level : DL ( $\times 10^{-6}$ W )	0.03	0.03	$DL = I_x^2 R_e < 1 \times 10^{-6} W, R_e = R_1 ( 1 + C_o / CL )^2$
Negative resistance : $ -RL $ ( kohm )	410	440	5 times larger than $R_{1MAX}$
Oscillation allowance : M ( times )	6.3	6.8	Judgemental standard of oscillation stability
Voltage of oscillation start : Vstart ( V )	1.60	1.60	
Voltage of oscillation stop : Vstop ( V )	1.59	1.59	
Oscillation start up time : Ts ( sec )	1.10	1.10	Time to reach 90% of output level

Temperature characteristics of circuit	Low(*1)	Normal(*2)	Remarks
at -40°C Variation : $df / T$ ( $\times 10^{-6}$ )	-130	-130	Typ.Tp=25°C ( K = $-3.5 \times 10^{-8} / ^\circ C^2$ )
at +85°C Variation : $df / T$ ( $\times 10^{-6}$ )	-127	-127	Typ.Tp=25°C ( K = $-3.5 \times 10^{-8} / ^\circ C^2$ )

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

\*1; low consumption current mode

\*2; normal current mode

### Seiko Instruments USA Inc.

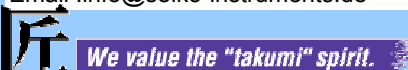
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Seiko Instruments Inc.  
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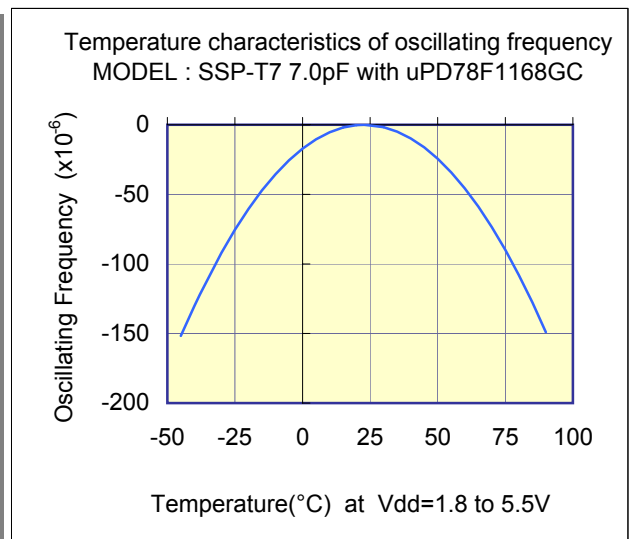
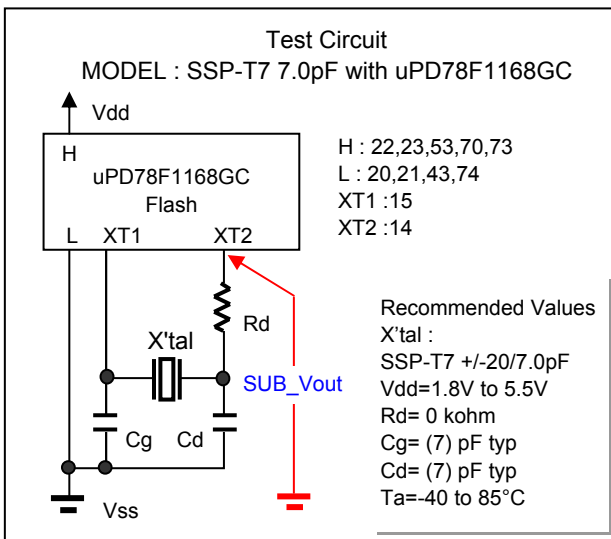
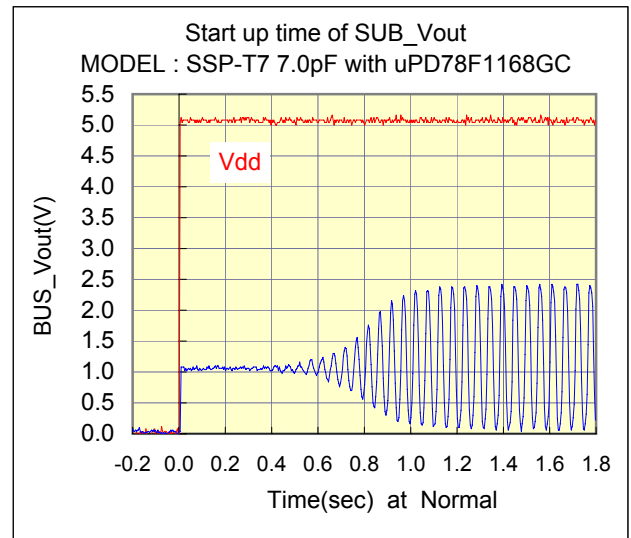
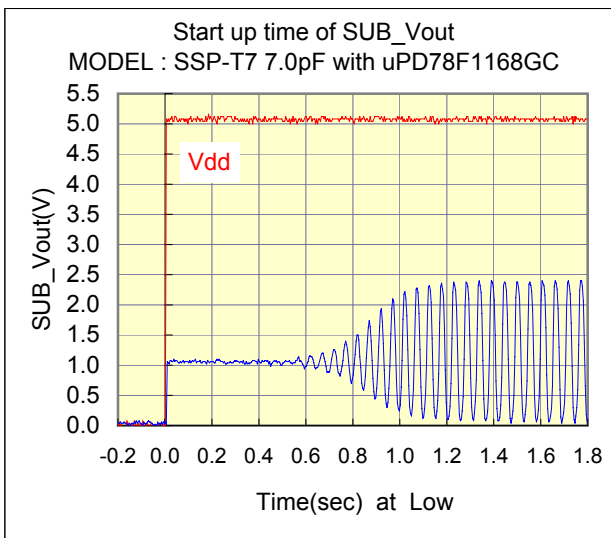
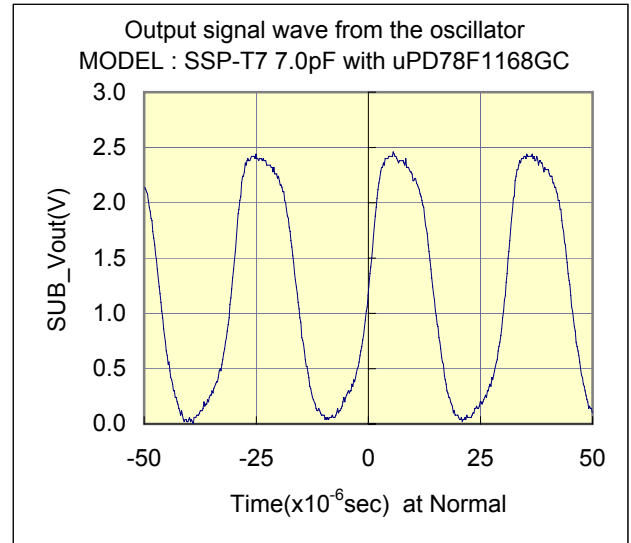
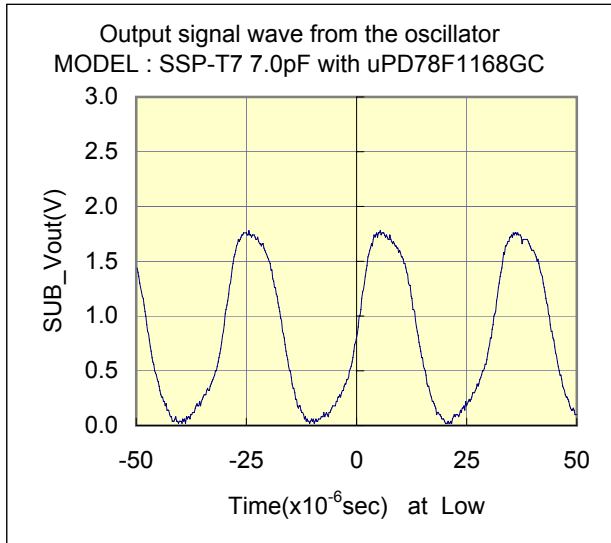
# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1168GC-16BT] LQFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



## Test Data at 25°C



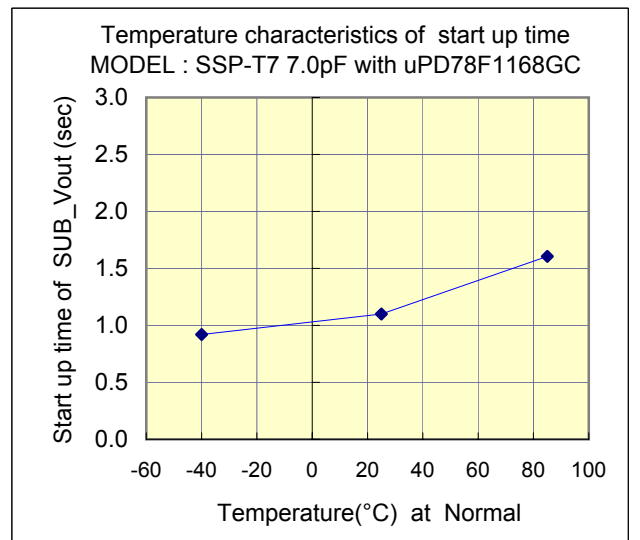
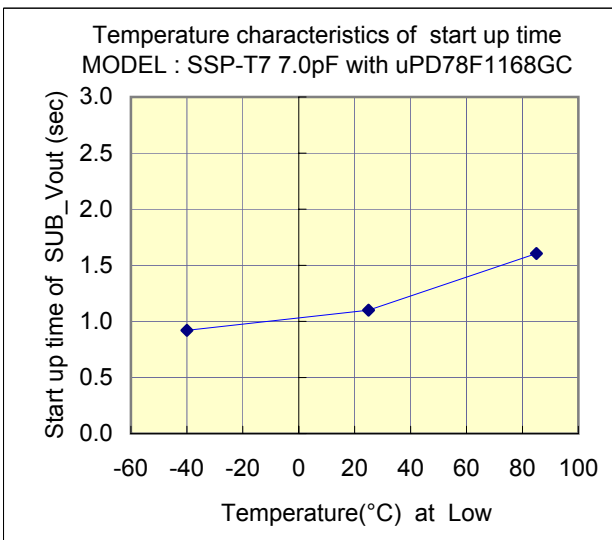
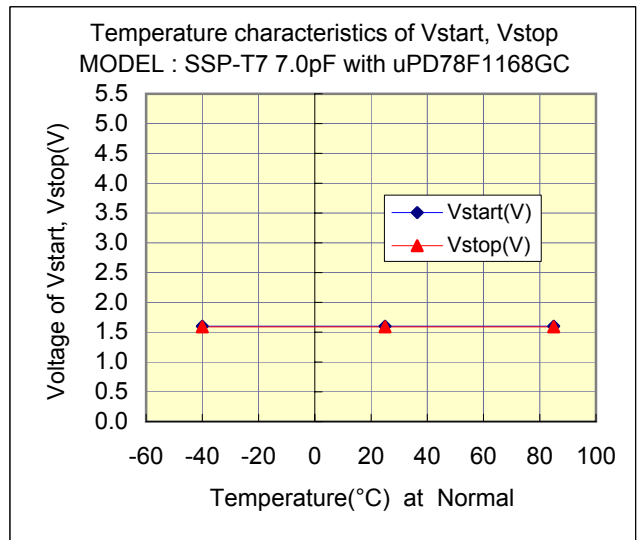
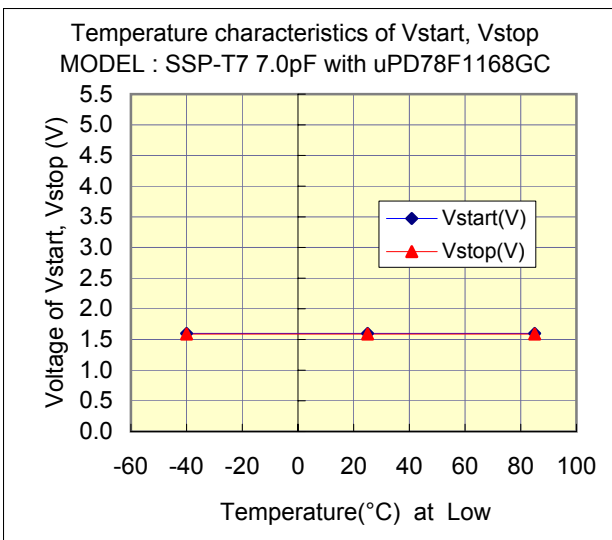
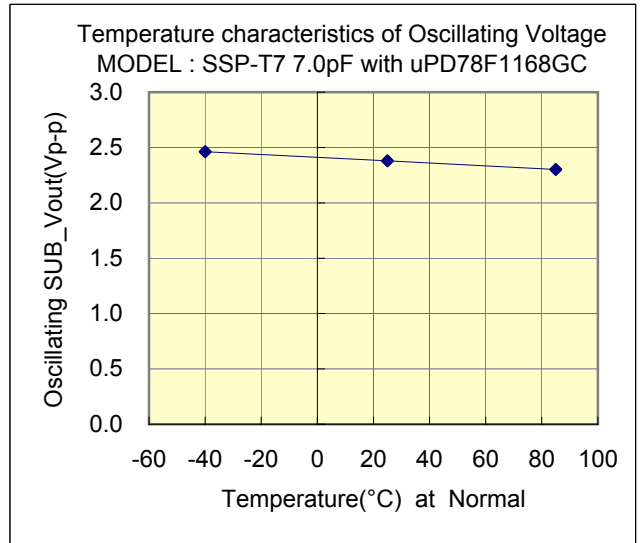
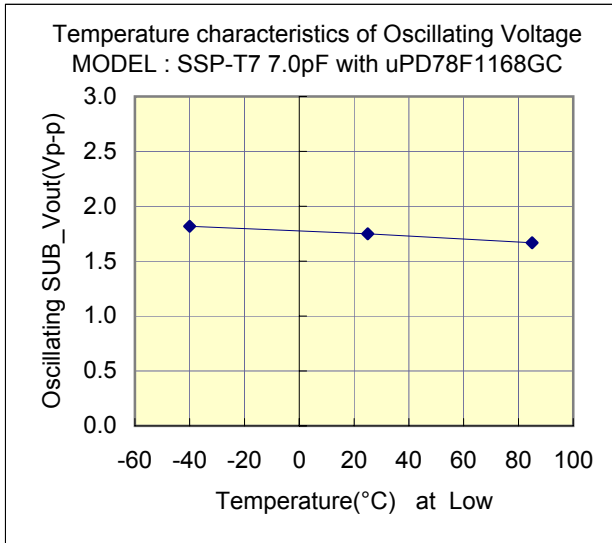
# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1168GC-16BT] LQFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



## Test Data : Temperature characteristics



# Evaluation of Subsystem Clock Oscillation Circuit

[ $\mu$ PD78F1168GC-16BT] LQFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



## Referential components layout(see Figure 1)

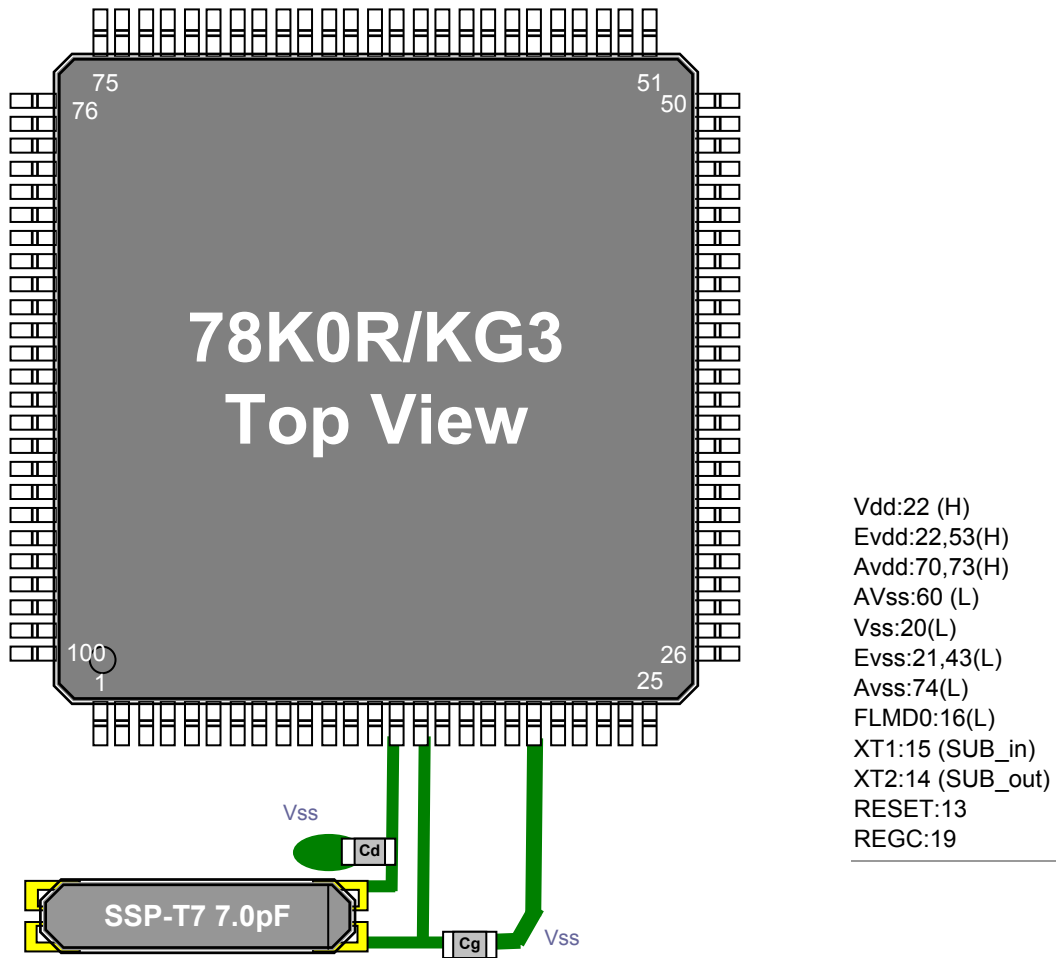


Figure 1 Referential components layout

## Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB\_in and SUB\_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

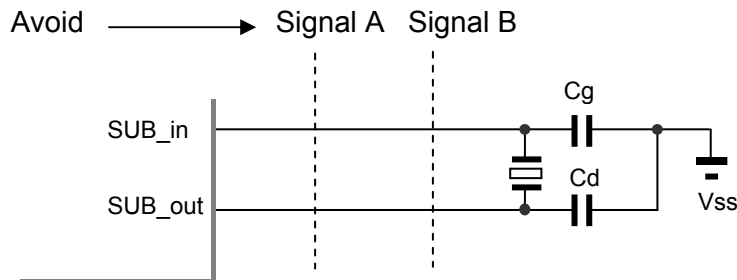


Figure 2 Example of Incorrect Board Design

**Remark** When using the subsystem clock, insert resistors  $R_d$  in series on the SUB\_out side.

# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1168GC-16BT] LQFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



## [Evaluation Sample : SSP-T7 7.0pF at 25°C]

SAMPLE	No.	CL (pF)	Fo (Hz)	fr (Hz)	R1 (kohm)	Co (pF)	C1 (fF)	Q (k)
SSP-T7 7.0pF	1	7	32768.40	32764.24	37.8	0.83	1.987	64.7
	2	7	32767.88	32763.63	39.2	0.85	2.037	60.9
	3	7	32767.98	32763.87	39.5	0.87	1.974	62.3

## [IC Test Data : IC Sample Rd=0ohm,Cg=7pF,Cd=7pF at 25°C]

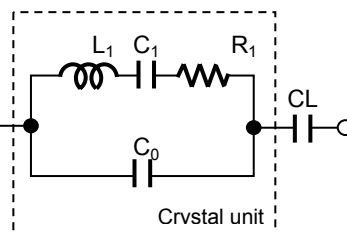
Mode	IC Sample	Fosc (Hz)	df / f (x10 <sup>-6</sup> )	DL(x10 <sup>-6</sup> W)	-RL  ( kohm)	Vstart (V)	Ts(sec)
Normal	TYP	32768.19	6.41	0.03	440	1.60	1.10
	HH	32768.12	4.27	0.04	440	1.60	1.16
	HL	32768.22	7.17	0.03	480	1.60	1.07
	LH	32768.09	3.36	0.04	440	1.60	1.13
	LL	32768.20	6.71	0.03	480	1.60	1.08

## [IC Test Data : IC Sample Rd=0ohm,Cg=7pF,Cd=7pF at 25°C]

Mode	IC Sample	Fosc (Hz)	df / f (x10 <sup>-6</sup> )	DL(x10 <sup>-6</sup> W)	-RL  ( kohm)	Vstart (V)	Ts(sec)
Low	TYP	32767.99	0.31	0.03	410	1.60	1.10
	HH	32767.92	-1.83	0.03	380	1.60	1.16
	HL	32768.00	0.61	0.03	410	1.60	1.07
	LH	32767.89	-2.75	0.03	380	1.60	1.13
	LL	32768.00	0.61	0.03	410	1.60	1.08

### Remark ( see figure 3 )

$$F_o = f_r \times \left\{ \frac{C_1}{2 \times (C_o + C_L)} + 1 \right\} \text{ ( Hz )}$$



Fo : Load resonance frequency  
 fr : Resonance frequency  
 R1 : Motional resistance  
 C1 : Motional capacitance  
 Co : Shunt capacitance  
 CL : Load Capacitance

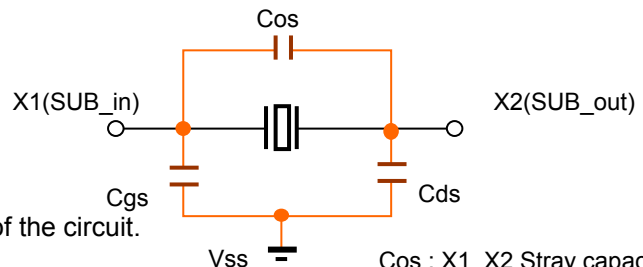
Figure 3 Equivalent circuit of crystal unit, and CL

### Remark ( see figure 4 )

Approximate formula of the load capacitance of the circuit CL.

$$CL = C_g \times C_d / (C_g + C_d) + C_s \text{ (pF)}$$

Where Cs(=2 to 4pF) Stands for stray capacitance of the circuit.



Cos : X1\_X2 Stray capacitance  
 Cgs : X1\_Vss Stray capacitance  
 Cds : X2\_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.



# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1168GC-16BT] LQFP(14x14) 0.50mm pitch

Measurement conditions : Vdd=1.6V to 6.0V at 25°C

## Referential Data : Voltage characteristics

