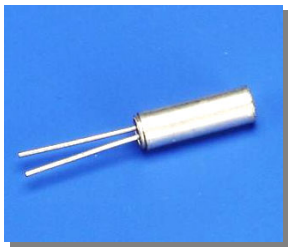
V850ES/JG3-L 24-Jul-08

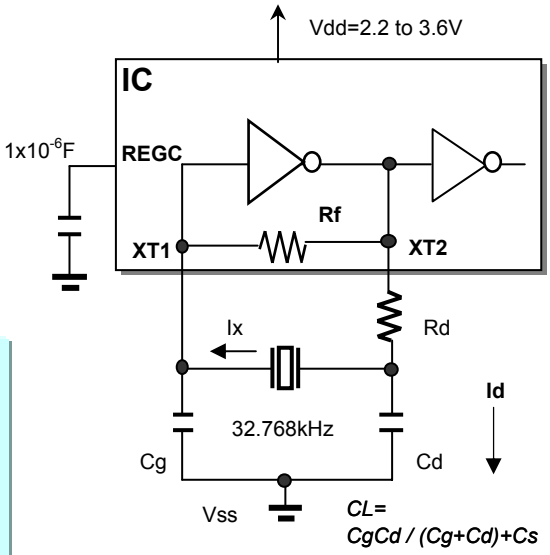
Evaluation of Subsystem Clock Oscillation Circuit

VT-200 6.0pF with uPD70F3738GC-32BT [LQFP(14x14) 0.50mm pitch]

Measurement conditions : 3.3V



Model	:VT-200
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10^{-6}
Load capacitance	:CL=6.0pF
Equivalent series resistance	:R1=50kohm max
Max. drive level	:DL=1x10^{-6}W max
Level of drive	:DL=0.1x10^{-6}W typ

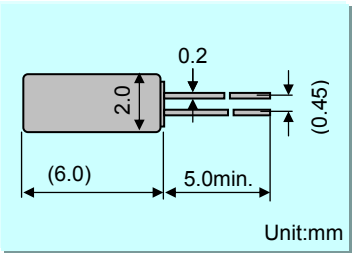


Remark) Ix : current through crystal

FEATURES

1.Compact tubular package
2.Photolithographic process
3.Excellent shock resistance and environmental characteristics.
4.Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)



MODEL:VT-200 6.0pF with uPD70F3738GC at 25°C

Key specifications	Low(*1)	Normal(*2)	Remarks
Current control resistance : Rd (k ohm)	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	6	6	Optimal capacitance in response to CL
Capacitance at drain : Cd (pF)	6	6	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Low(*1)	Normal(*2)	Remarks
Matching Accuracy : df / f (x10^{-6})	-0.7	5.3	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V (x10^{-6})	0.0	0.0	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL (x10^{-6}W)	0.02	0.02	DL=Ix^2 Re < 1x10^{-6}W,Re=R1(1 + Co / CL)^2
Negative resistance : | - RL | (kohm)	597	857	5 times larger than R_{1MAX}
Oscillation allowance : M (times)	12	17	Judgemental standard of oscillation stability
consumption current : Id (nA)	646	822	Cd charge current, Id = ωCd*Vd
Voltage of oscillation start : Vstart (V)	1.04	1.04	
Voltage of oscillation stop : Vstop (V)	0.97	0.97	
Oscillation start up time : Ts (sec)	0.70	0.70	Time to reach 90% of output level

Temperature characteristics of circuit		Low(*1)	Normal(*2)	Remarks
at -40°C	Variation : df / T (x10^{-6})	-141	-141	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^2)
at +85°C	Variation : df / T (x10^{-6})	-124	-124	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^2)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

*1; low consumption current mode

*2; normal current mode

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Evaluation of Subsystem Clock Oscillation Circuit

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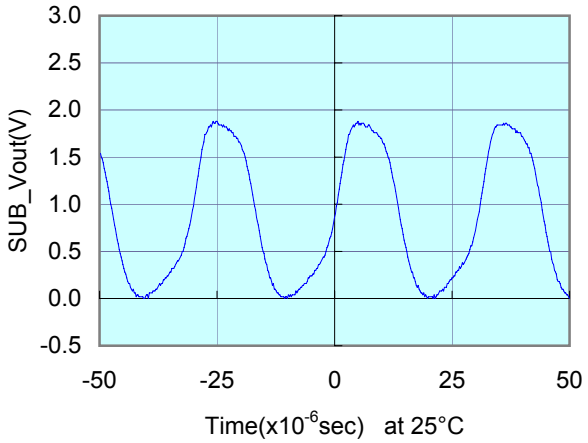
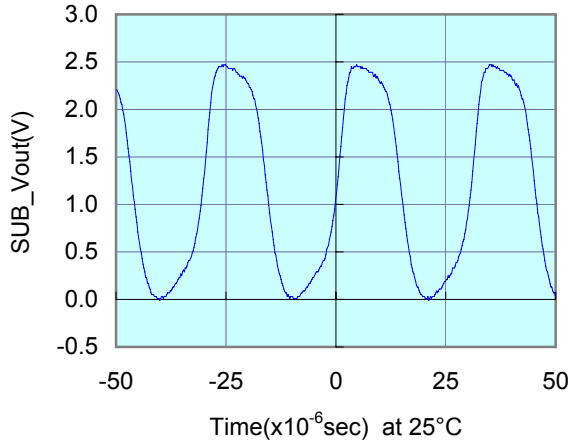
Measurement conditions : 3.3V

Test Data

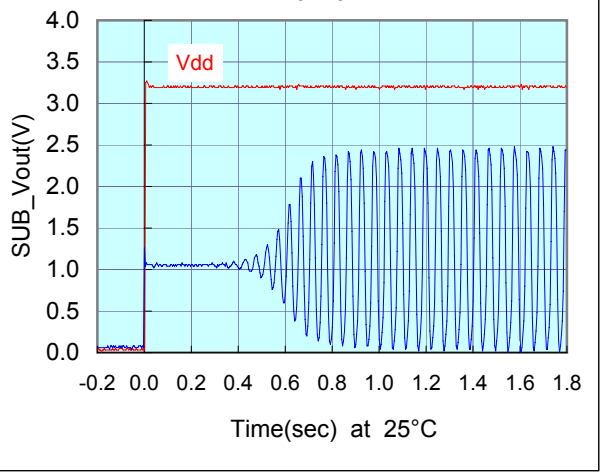
Output signal wave from the oscillator
Low



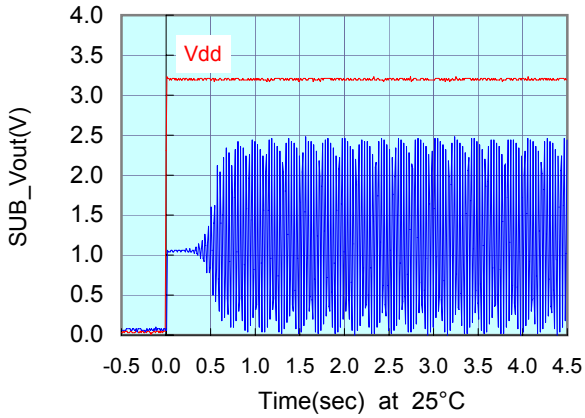
Output signal wave from the oscillator
Normal



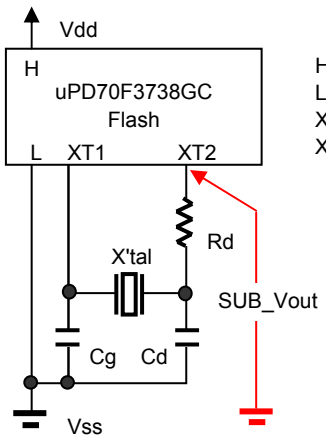
Start up time of SUB_Vout(1)
Normal



Start up time of SUB_Vout(2)
Normal

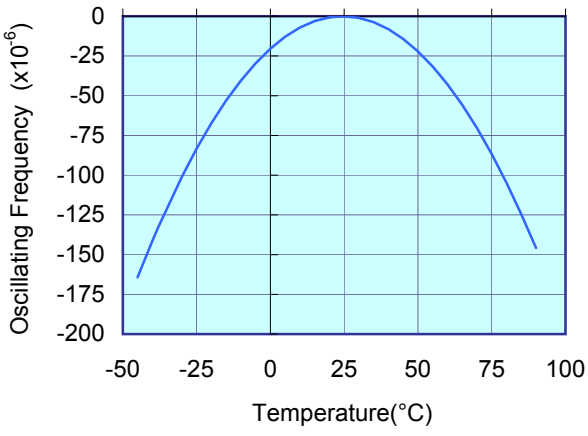


Test Circuit



H : 1,5,9,34,70
L : 2,11,33,69
XT1 :15
XT2 :16

Temperature characteristics of oscillating frequency



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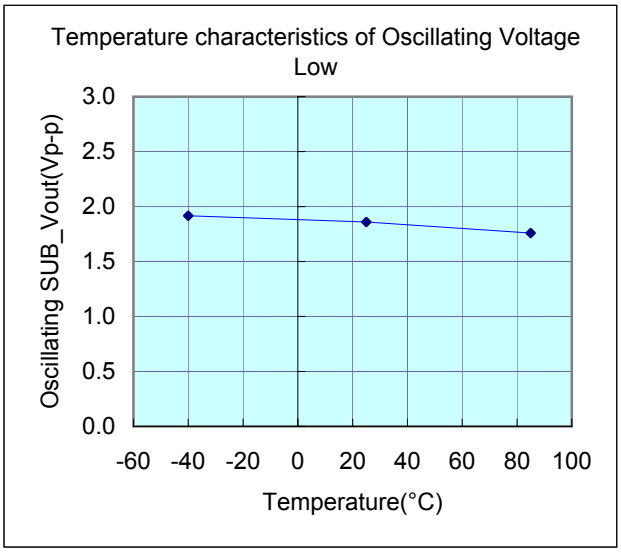
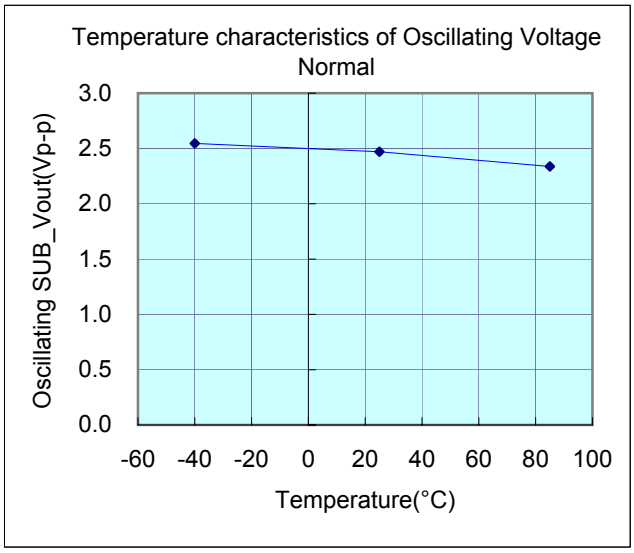
Evaluation of Subsystem Clock Oscillation Circuit

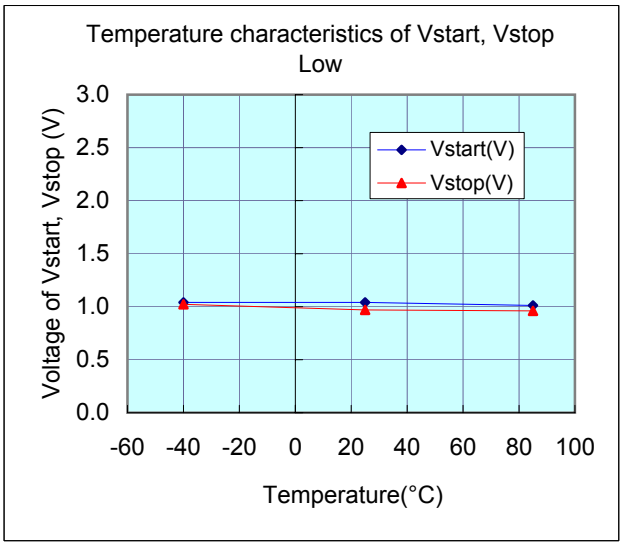
VT-200 6.0pF with uPD70F3738GC-32BT [LQFP(14x14) 0.50mm pitch]

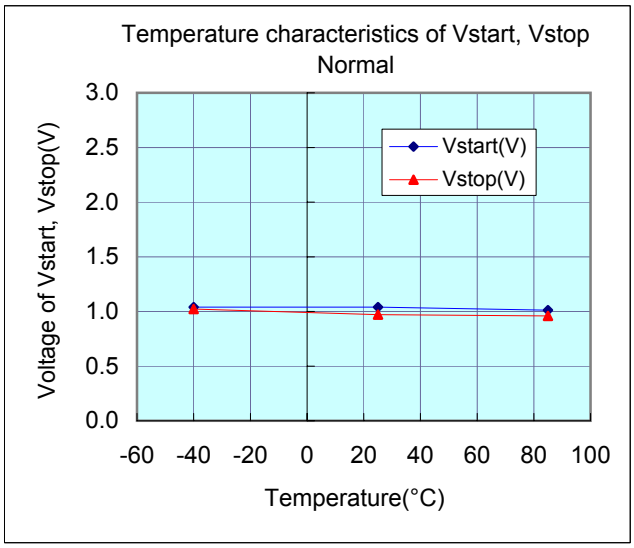
Measurement conditions : 3.3V

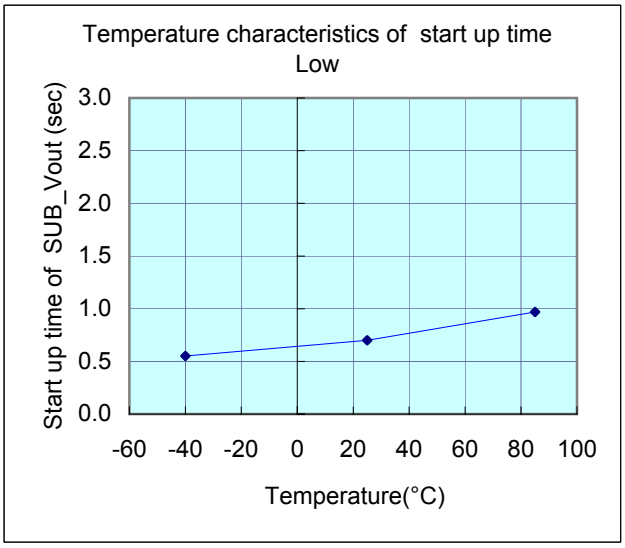
Test Data : Temperature characteristics

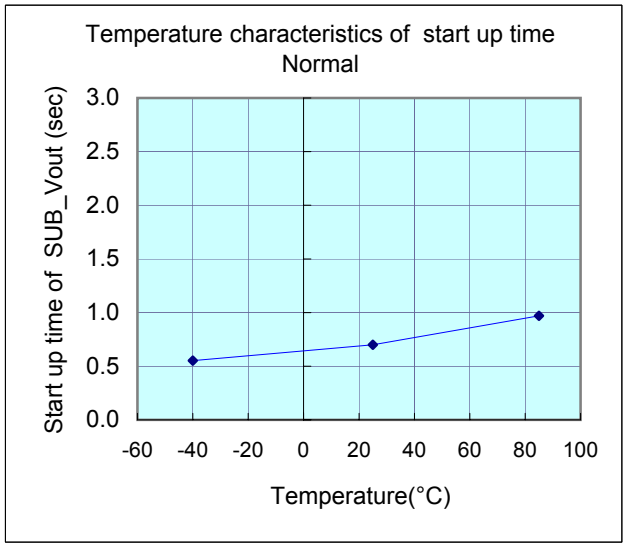












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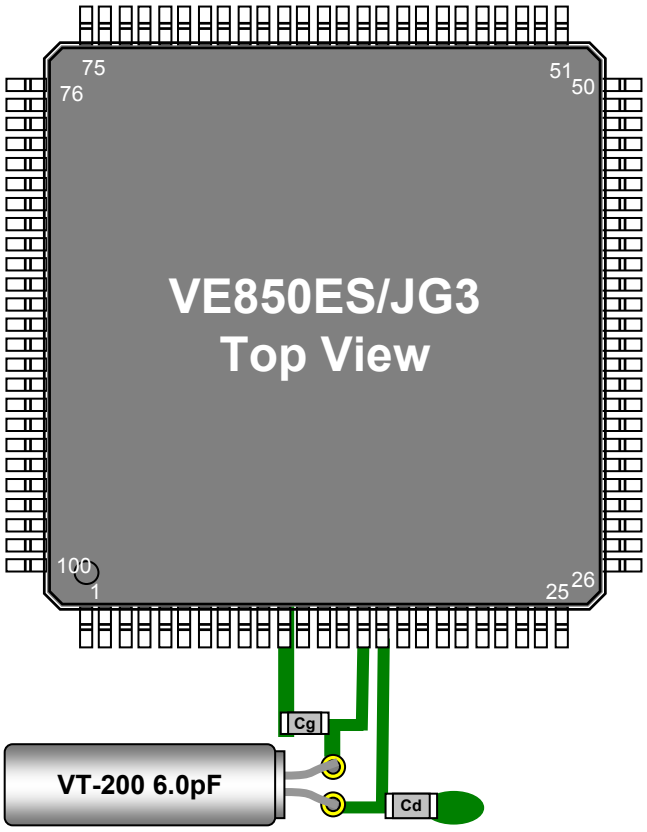
Evaluation of Subsystem Clock Oscillation Circuit

VT-200 6.0pF with uPD70F3738GC-32BT [LQFP(14x14) 0.50mm pitch]

Measurement conditions : 3.3V

Referential components layout(see Figure 1)



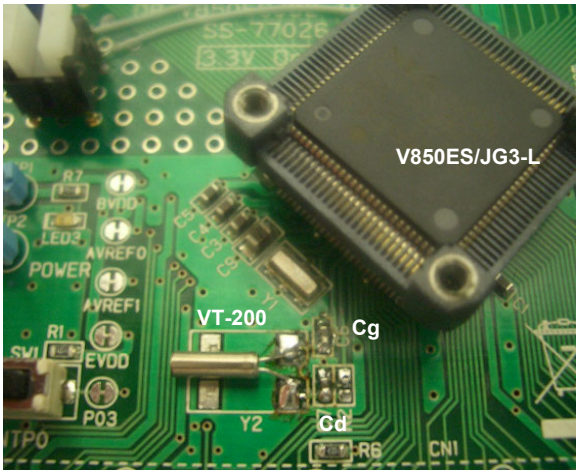


Figure 1 Referential components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.
Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

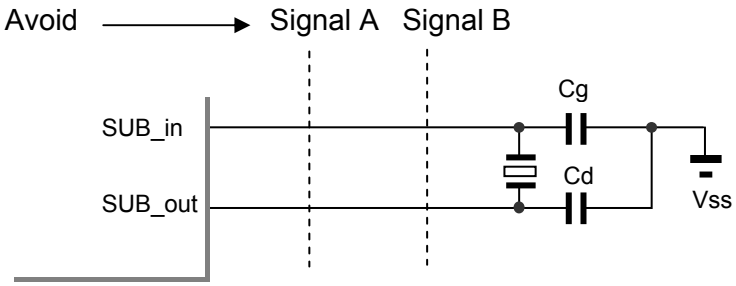


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert resistors Rd in series on the SUB_out side.

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Measurement conditions : 3.3V

[Evaluation Sample at 25°C]

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
VT-200 6.0pF	1	6	32768.01	32762.79	28.0	0.90	2.199	78.9
	2	6	32767.89	32762.71	27.6	0.90	2.182	80.7
	3	6	32768.10	32762.84	27.1	0.90	2.216	80.9

[IC Test Data : IC Sample Rd=0ohm,Cg=6pF,Cd=6pF at 25°C]

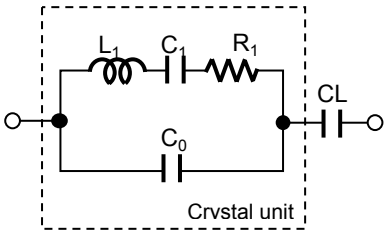
Mode	IC Sample	Fosc(Hz)	df / f(x10^{-6})	DL(x10^{-6}W)	| -RL |(kohm)	Id (nA)	Vstart(V)	Ts(sec)
Normal	TYP	32768.19	5.34	0.02	857	822	1.04	0.70
	HH	32768.11	2.96	0.03	787	846	1.17	0.85
	HL	32768.19	5.37	0.02	857	832	0.99	0.69
	LH	32768.12	3.42	0.02	787	840	1.16	0.76
	LL	32768.21	6.23	0.02	947	817	0.98	0.69

[IC Test Data : IC Sample Rd=0ohm,Cg=6pF,Cd=6pF at 25°C]

Mode	IC Sample	Fosc(Hz)	df / f(x10^{-6})	DL(x10^{-6}W)	| -RL |(kohm)	Id (nA)	Vstart(V)	Ts(sec)
Low	TYP	32767.99	-0.67	0.02	597	646	1.04	0.70
	HH	32767.93	-2.59	0.02	547	659	1.17	0.85
	HL	32767.98	-0.82	0.02	597	650	0.99	0.69
	LH	32767.93	-2.32	0.02	547	654	1.16	0.76
	LL	32768.01	0.00	0.02	657	646	0.98	0.69

Remark (see figure 3)

$$Fo = fr \times \{ C1 / (2 \times (Co + CL)) + 1 \} \quad (Hz)$$



Fo : Load resonance frequency
fr : Resonance frequency
R1 : Motional resistance
C1 : Motional capacitance
Co : Shunt capacitance
CL : Load Capacitance

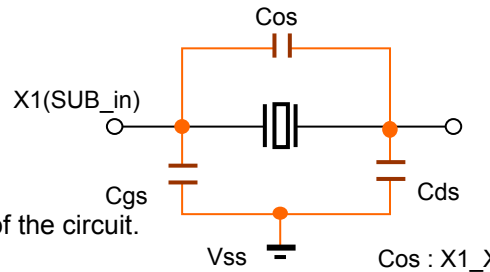
Figure 3 Equivalent circuit of crystal unit, and CL

Remark (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

$$CL = Cg \times Cd / (Cg + Cd) + Cs \quad (pF)$$

Where Cs(=2 to 4pF) Stands for stray capacitance of the circuit.



Cos : X1_X2 Stray capacitance
Cgs : X1_Vss Stray capacitance
Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

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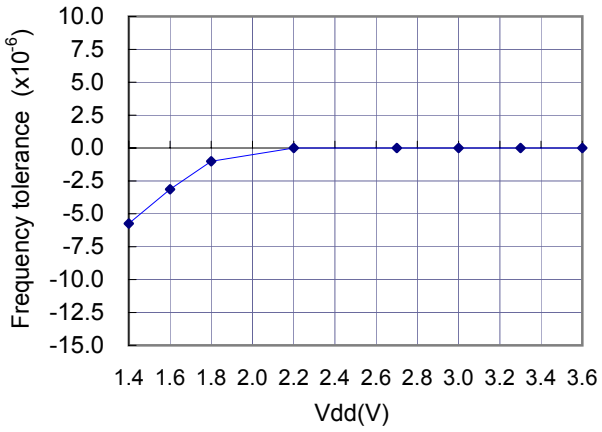
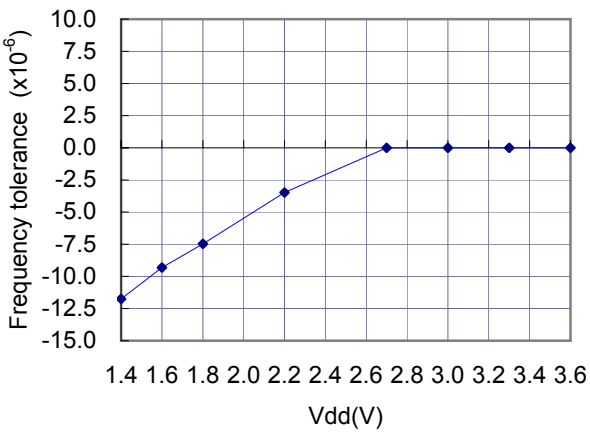
Measurement conditions : Vdd=(1.4V) to 3.6V at 25°C

Referential Data : Voltage characteristics

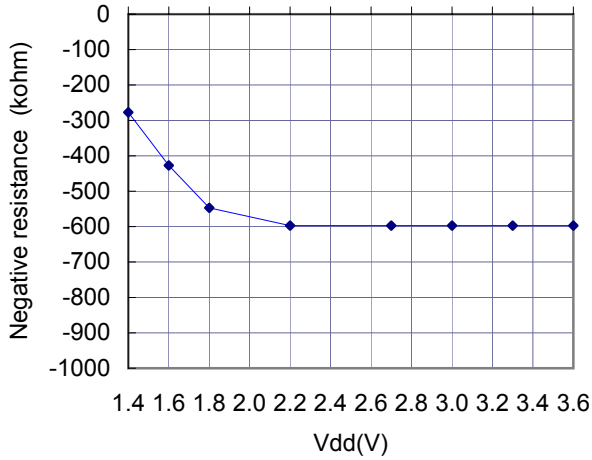
Frequency / voltage coefficient
Low



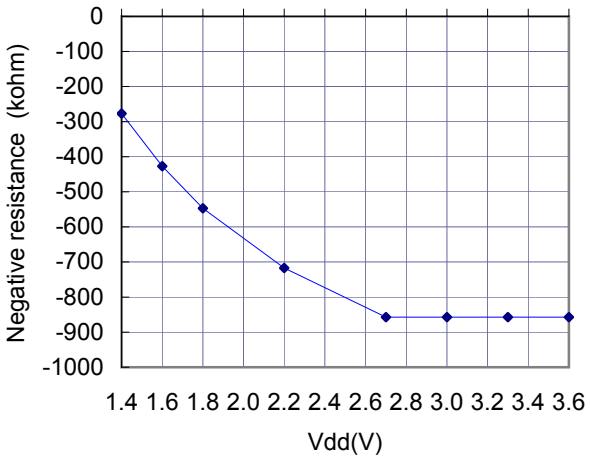
Frequency / voltage coefficient
Normal



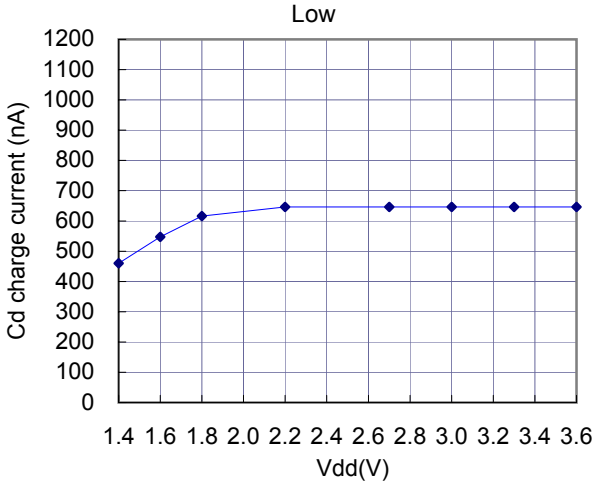
Negative resistance / voltage coefficient
Low



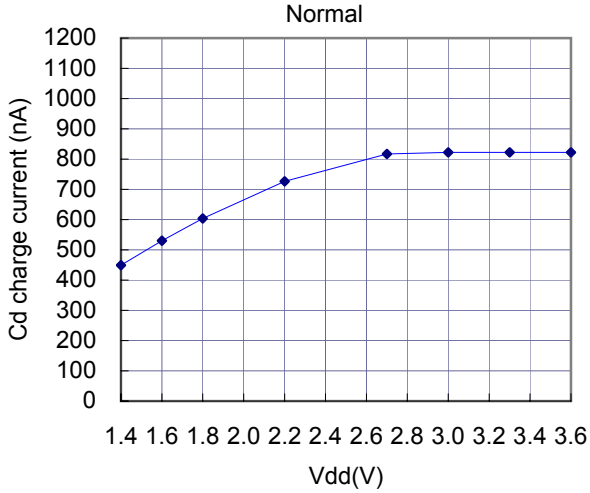
Negative resistance / voltage coefficient
Normal



Cd charge current / voltage coefficient
Low



Cd charge current / voltage coefficient
Normal



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