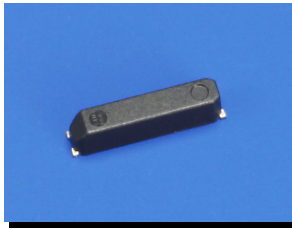


Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7 7.0pF with uPD70F3738GC-32BT [LQFP(14x14) 0.50mm pitch]

Measurement conditions : 3.3V

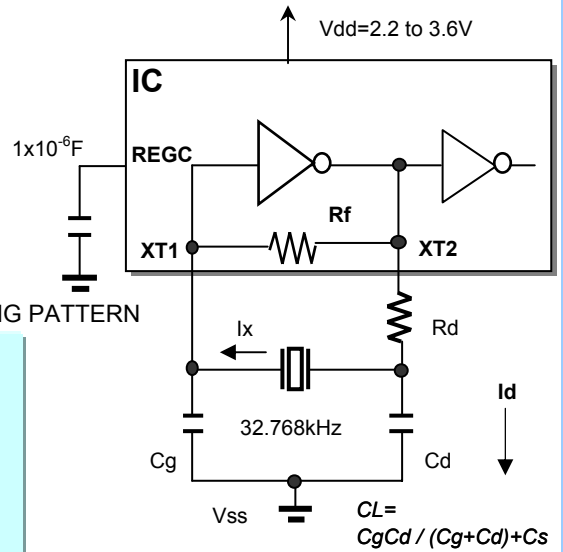
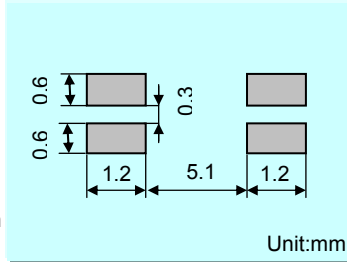


Model : SSP-T7  
 Frequency : Fo=32.768kHz  
 Frequency tolerance : dF/Fo= +/-20x10<sup>-6</sup>  
 Load capacitance : CL=7.0pF  
 Equivalent series resistance : R1=65kohm max  
 Max. drive level : DL=1x10<sup>-6</sup>W max  
 Level of drive : DL=0.1x10<sup>-6</sup>W typ

FEATURES

- 1.Ultra thin type with 1.4mm Max.
- 2.SMD type suitable for automatic & high density surface mounting.
- 3.Plastic mold package containing highly reliable tubular type quartz crystal.
- 4.Excellent shock and heat resistance.
- 5.Cellular phones,PDA,Radio communication equipment, Portable applications etc.

RECOMMENDED SOLDERING PATTERN



Remark) Ix : current through crystal

MODEL:SSP-T7 7.0pF with uPD70F3738GC at 25°C

Key specifications	Low(*1)	Normal(*2)	Remarks
Current control resistance : Rd ( k ohm )	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg ( pF )	8	8	Optimal capacitance in response to CL
Capacitance at drain : Cd ( pF )	8	8	( CL = Cd // Cg + stray capacitance )

Circuit characteristics ( at 25°C )	Low(*1)	Normal(*2)	Remarks
Matching Accuracy : df / f ( x10 <sup>-6</sup> )	1.2	5.5	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V ( x10 <sup>-6</sup> )	0.0	0.0	Vdd +/-10% ( Standard operating voltage range )
Drive Level : DL ( x10 <sup>-6</sup> W )	0.05	0.05	DL=Ix <sup>2</sup> Re < 1x10 <sup>-6</sup> W, Re=R1( 1 + Co / CL ) <sup>2</sup>
Negative resistance :   - RL   ( kohm )	520	800	5 times larger than R1MAX
Oscillation allowance : M ( times )	8	12	Judgemental standard of oscillation stability
consumption current : Id (nA)	730	938	Cd charge current, Id = ωCd*Vd
Voltage of oscillation start : Vstart ( V )	1.08	1.08	
Voltage of oscillation stop : Vstop ( V )	1.00	1.00	
Oscillation start up time : Ts ( sec )	0.70	0.70	Time to reach 90% of output level

Temperature characteristics of circuit	Low(*1)	Normal(*2)	Remarks
at -40°C Variation : df / T ( x10 <sup>-6</sup> )	-139	-139	Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> )
at +85°C Variation : df / T ( x10 <sup>-6</sup> )	-128	-129	Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> )

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

\*1; low consumption current mode

\*2; normal current mode

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Seiko Instruments Inc.

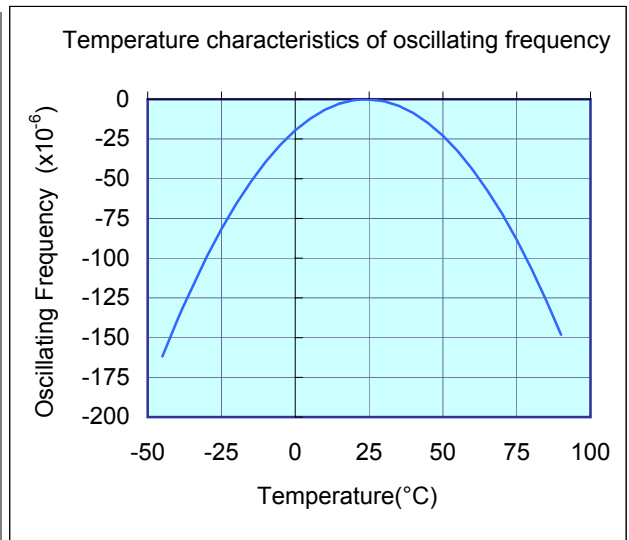
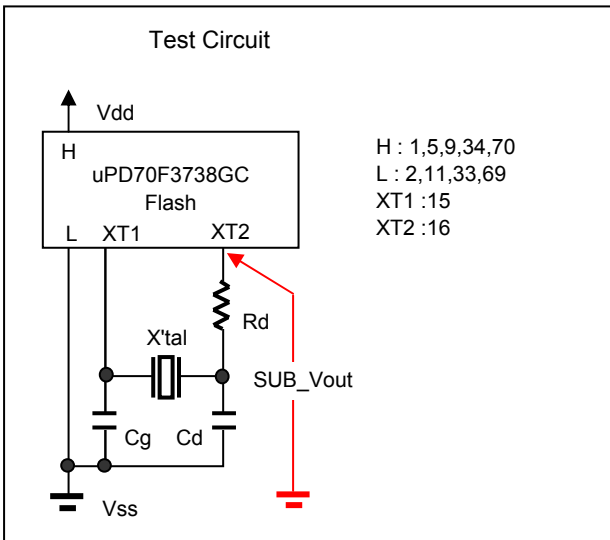
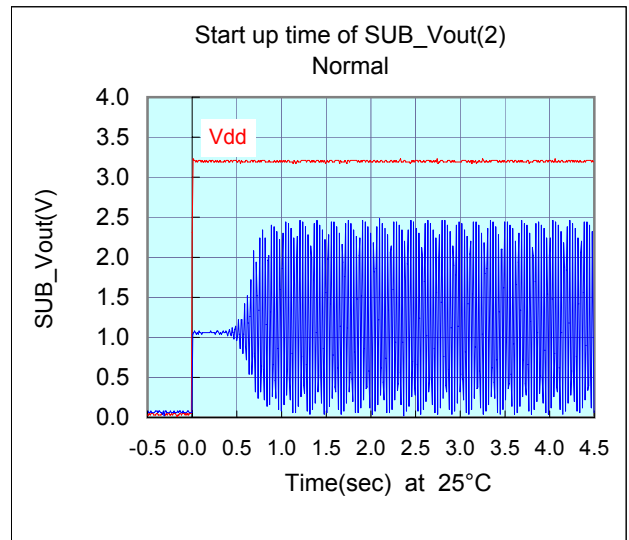
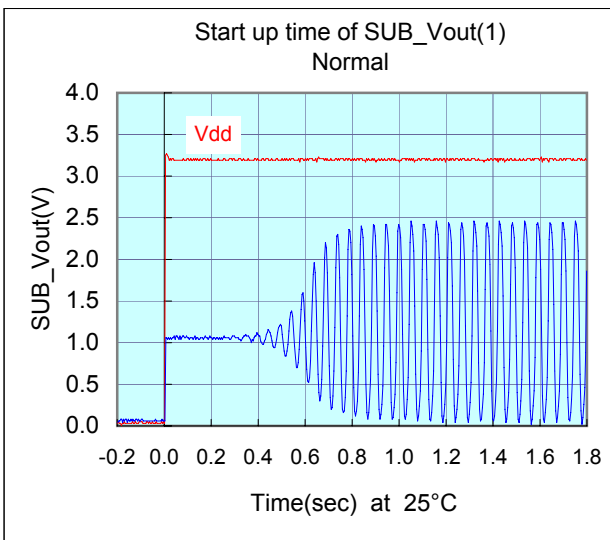
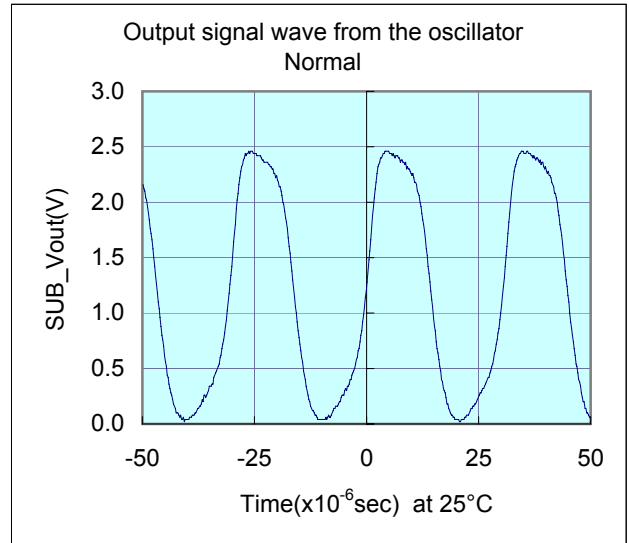
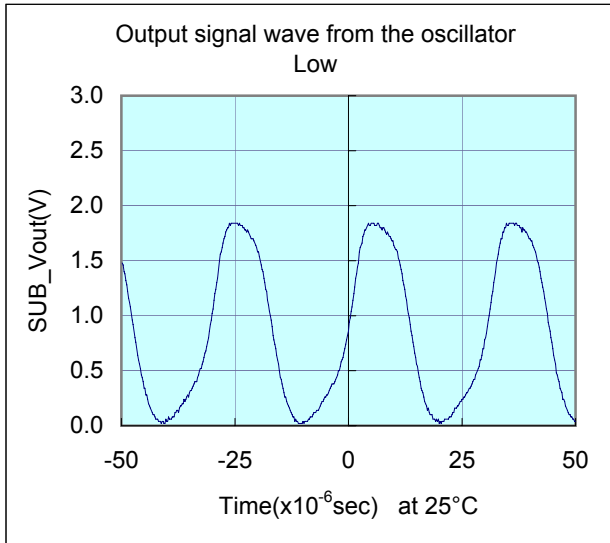
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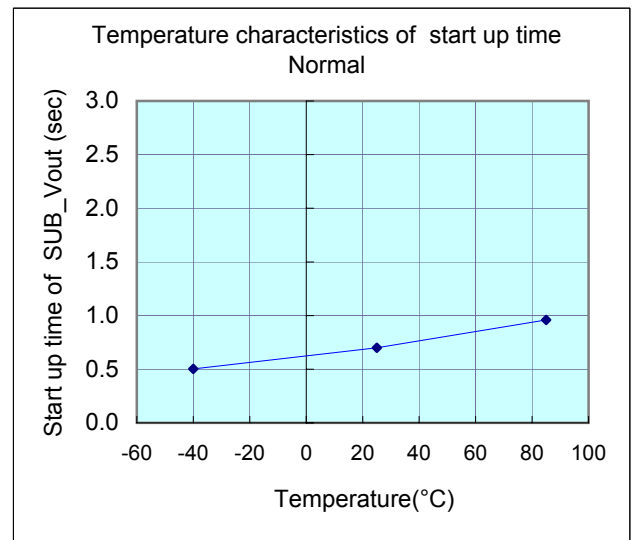
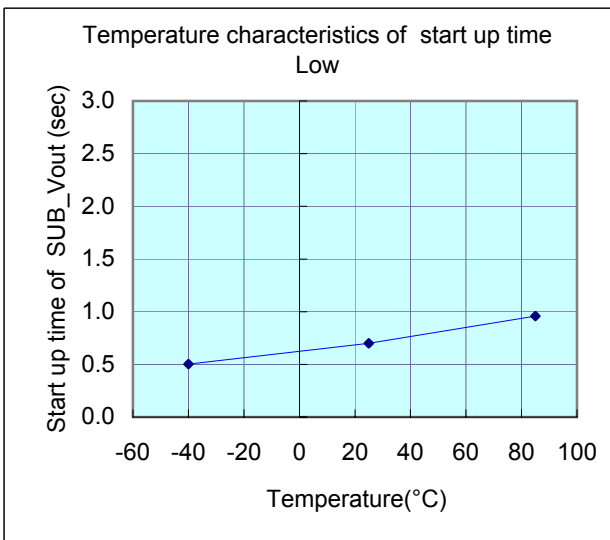
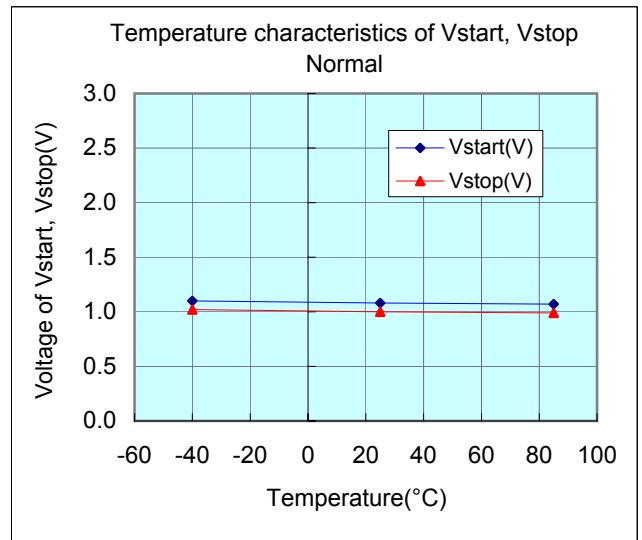
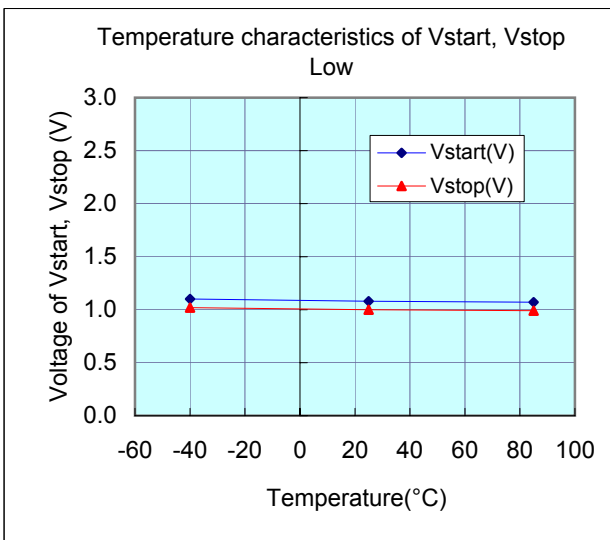
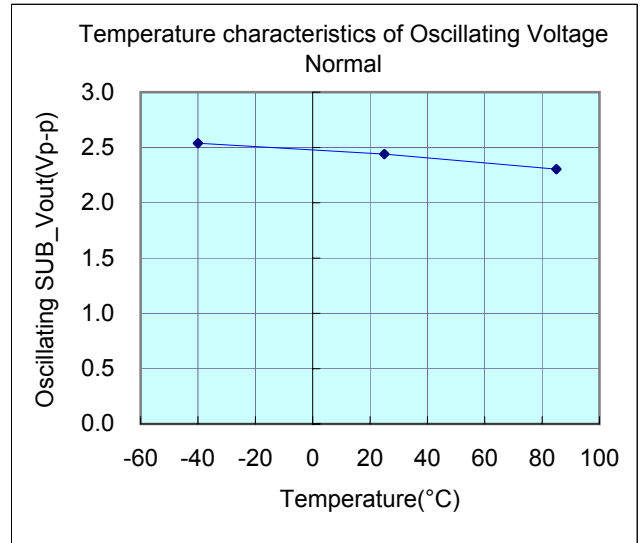
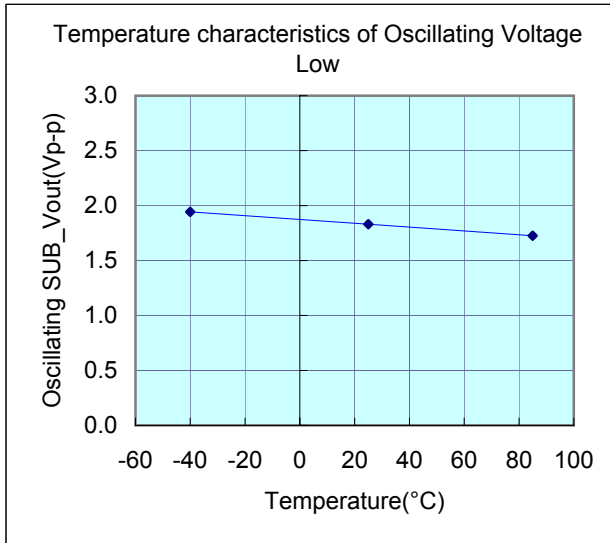
We value the "takumi" spirit.

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Test Data



Test Data : Temperature characteristics



Referential components layout(see Figure 1)

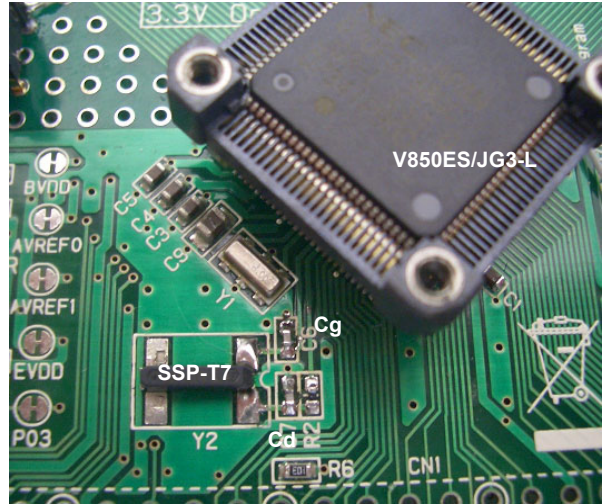
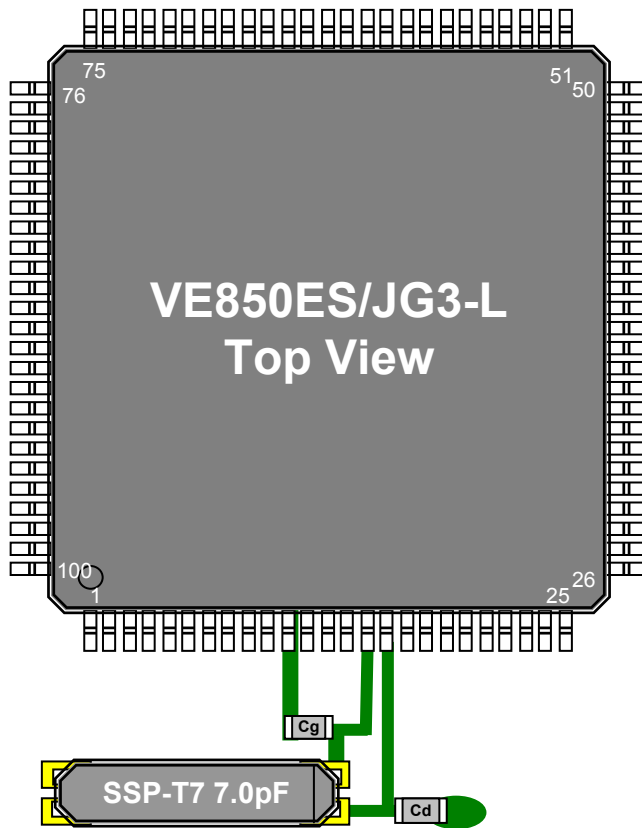


Figure 1 Referential components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB\_in and SUB\_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

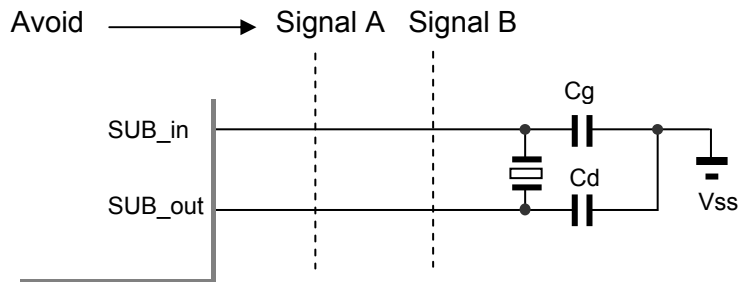


Figure 2 Example of Incorrect Board Design

**Remark** When using the subsystem clock, insert resistors Rd in series on the SUB\_out side.

Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7 7.0pF with uPD70F3738GC-32BT [LQFP(14x14) 0.50mm pitch]

Measurement conditions : 3.3V



[Evaluation Sample at 25°C]

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
SSP-T7 7.0pF	1	7	32768.40	32764.24	37.8	0.83	1.987	64.7
	2	7	32767.94	32763.77	40.5	0.85	1.998	60.1
	3	7	32768.10	32763.95	40.0	0.84	1.986	61.2

[IC Test Data : IC Sample Rd=0ohm,Cg=8pF,Cd=8pF at 25°C]

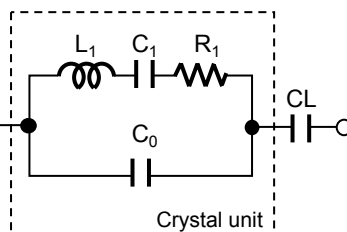
Mode	IC Sample	Fosc(Hz)	df / f( x10 <sup>-6</sup> )	DL(x10 <sup>-6</sup> W)	-RL  ( kohm)	Id (nA)	Vstart( V )	Ts(sec)
Normal	TYP	32768.28	5.49	0.05	800	938	1.08	0.70
	HH	32768.24	4.27	0.06	730	964	1.20	0.91
	HL	32768.29	5.80	0.05	800	944	1.02	0.75
	LH	32768.27	5.19	0.06	730	948	1.22	0.96
	LL	32768.32	6.71	0.05	800	932	1.00	0.74

[IC Test Data : IC Sample Rd=0ohm,Cg=8pF,Cd=8pF at 25°C]

Mode	IC Sample	Fosc(Hz)	df / f( x10 <sup>-6</sup> )	DL(x10 <sup>-6</sup> W)	-RL  ( kohm)	Id (nA)	Vstart( V )	Ts(sec)
Low	TYP	32768.14	1.22	0.05	520	730	1.08	0.70
	HH	32768.10	0.00	0.05	480	742	1.20	0.91
	HL	32768.15	1.53	0.04	520	724	1.02	0.75
	LH	32768.12	0.61	0.05	410	730	1.22	0.96
	LL	32768.17	2.14	0.04	560	720	1.00	0.74

Remark ( see figure 3 )

$$F_o = f_r \times \{ C_1 / ( 2 \times ( C_o + C_L ) ) + 1 \} \text{ ( Hz )}$$



- Fo : Load resonance frequency
- fr : Resonance frequency
- R1 : Motional resistance
- C1 : Motional capacitance
- Co : Shunt capacitance
- CL : Load Capacitance

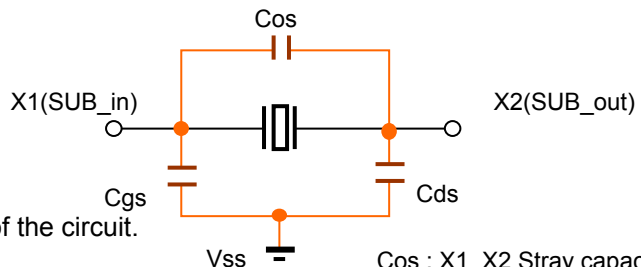
Figure 3 Equivalent circuit of crystal unit, and CL

Remark ( see figure 4 )

Approximate formula of the load capacitance of the circuit CL.

$$CL = C_g \times C_d / ( C_g + C_d ) + C_s \text{ ( pF )}$$

Where Cs(=2 to 4pF) Stands for stray capacitance of the circuit.



- Cos : X1\_X2 Stray capacitance
- Cgs : X1\_Vss Stray capacitance
- Cds : X2\_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7 7.0pF with uPD70F3738GC-32BT [LQFP(14x14) 0.50mm pitch]

Measurement conditions : Vdd=(1.6V) to 3.6V at 25°C



Referential Data : Voltage characteristics

