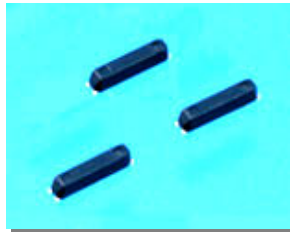


# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1166GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V

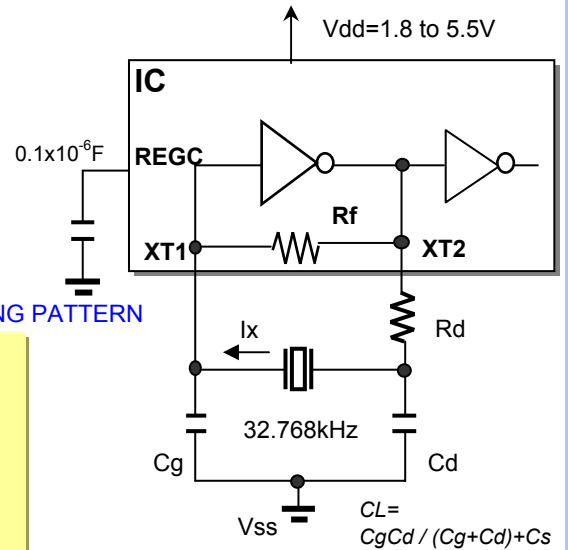
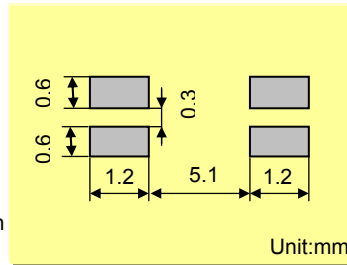


Model :SSP-T7  
 Frequency :Fo=32.768kHz  
 Frequency tolerance :dF/Fo= +/-20x10<sup>-6</sup>  
 Load capacitance :CL=12.5pF  
 Equivalent series resistance :R1=65kohm max  
 Max. drive level :DL=1x10<sup>-6</sup>W max  
 Level of drive :DL=0.1x10<sup>-6</sup>W typ

## FEATURES

- 1.Ultra thin type with 1.4mm Max.
- 2.SMD type suitable for automatic & high density surface mounting.
- 3.Plastic mold package containing highly reliable tubular type quartz crystal.
- 4.Excellent shock and heat resistance.
- 5.Cellular phones,PDA,Radio communication equipment, Portable applications etc.

## RECOMMENDED SOLDERING PATTERN

Remark) I<sub>x</sub> : current through crystal

MODEL:SSP-T7 12.5pF with uPD78F1166GC at 25°C

Key specifications	Low	High	Remarks
Current control resistance : Rd ( k ohm )	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg ( pF )	10	10	Optimal capacity in response to CL
Capacitance at drain : Cd ( pF )	10	10	( CL = Cd // Cg + stray capacitance )

Circuit characteristics ( at 25°C )	Low	High	Remarks
Matching Accuracy : df / f ( x10 <sup>-6</sup> )	0.2	3.1	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V ( x10 <sup>-6</sup> )	0.0	0.0	Vdd +/-10% ( Standard operating voltage range )
Drive Level : DL ( x10 <sup>-6</sup> W )	0.13	0.26	DL=I <sub>x</sub> <sup>2</sup> Re < 1x10 <sup>-6</sup> W, Re=R1( 1 + Co / CL ) <sup>2</sup>
Negative resistance :   - RL   ( kohm )	174	284	5 times larger than R <sub>1MAX</sub>
Oscillation allowance : M ( times )	2.7	4.4	Judgemental standard of oscillation stability
Voltage of oscillation start : Vstart ( V )	1.61	1.61	
Voltage of oscillation stop : Vstop ( V )	1.59	1.59	
Oscillation start up time : Ts ( sec )	1.50	1.50	Time to reach 90% of output level

Temperature characteristics of circuit	Low	High	Remarks
at -40°C Variation : df / T ( x10 <sup>-6</sup> )	-129	-129	Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> )
at +85°C Variation : df / T ( x10 <sup>-6</sup> )	-132	-132	Typ.Tp=25°C ( K = -3.5x10 <sup>-8</sup> / °C <sup>2</sup> )

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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We value the "takumi" spirit.

Seiko Instruments Inc.  
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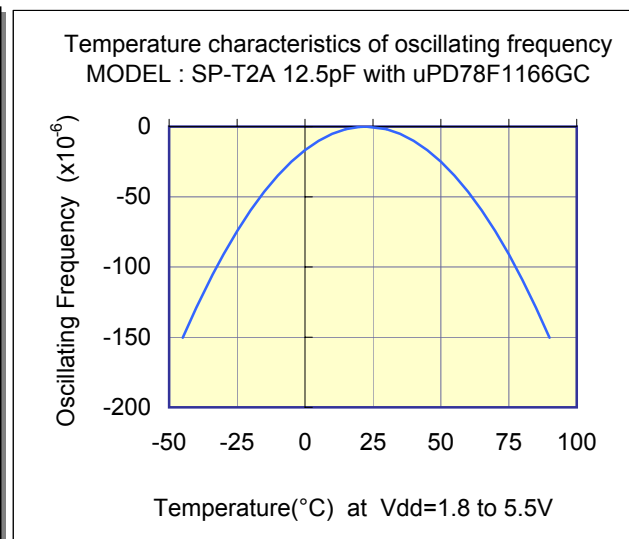
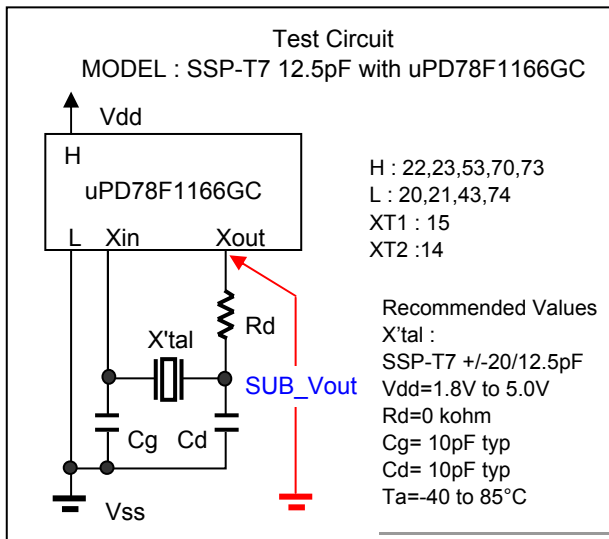
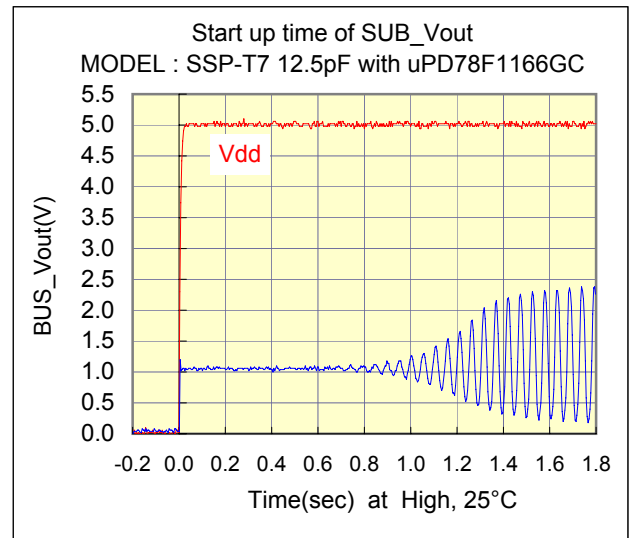
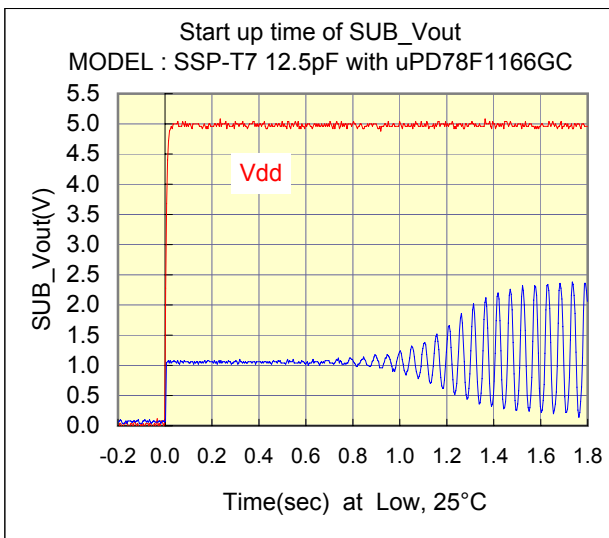
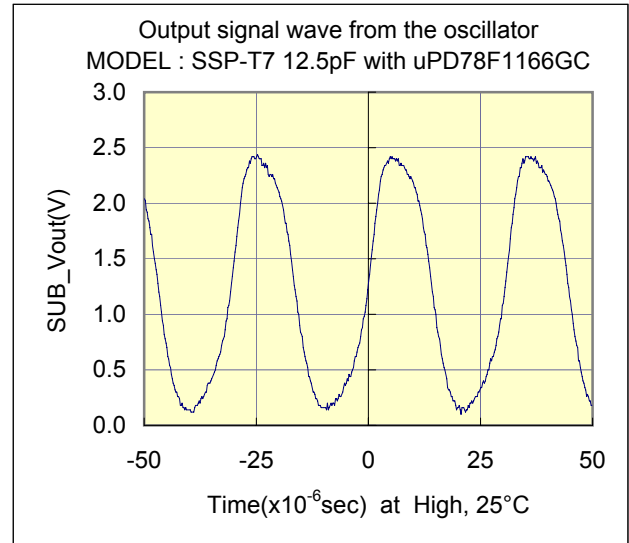
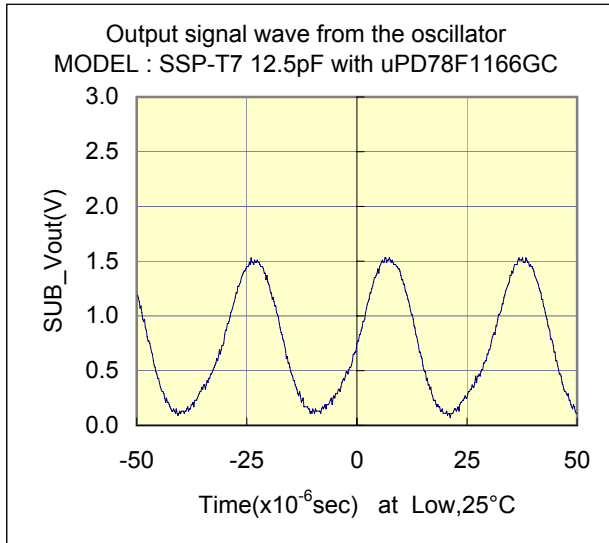
# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1166GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



## Test Data



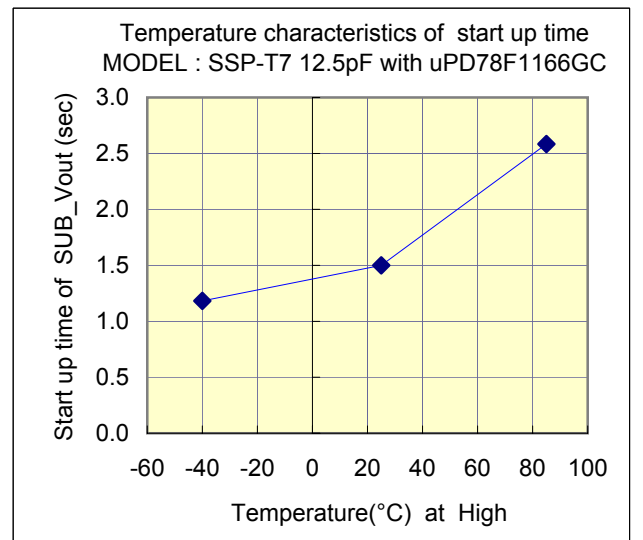
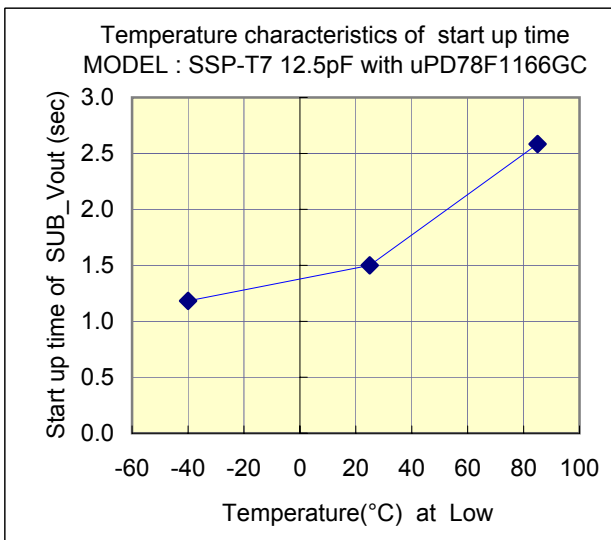
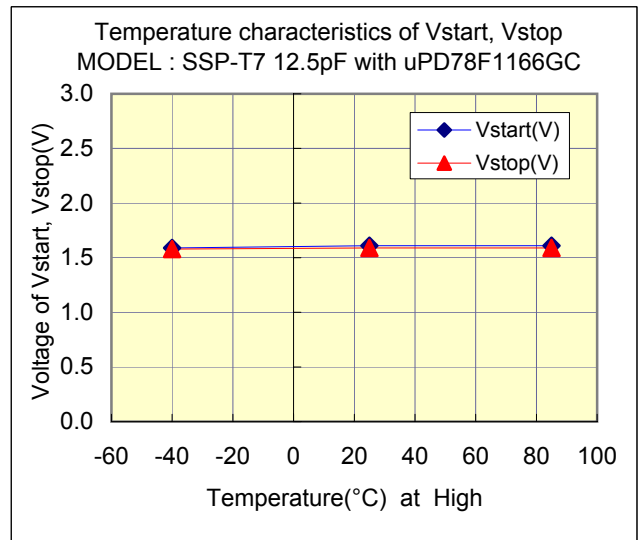
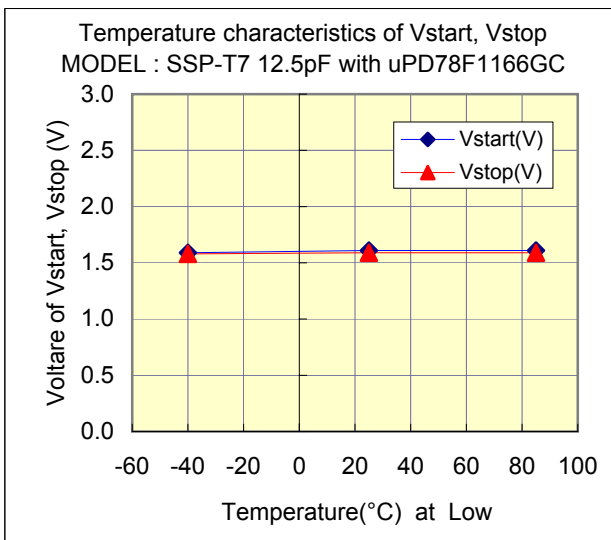
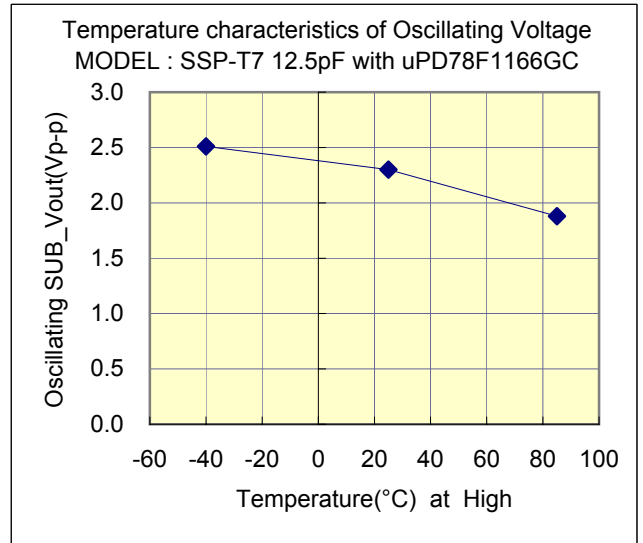
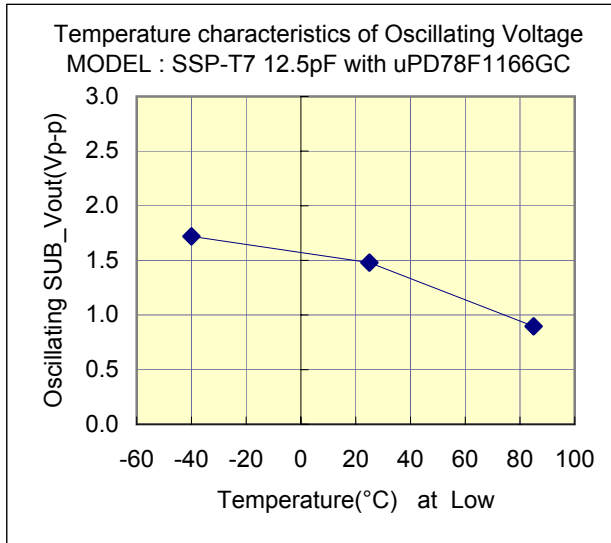
# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1166GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



## Test Data : Temperature characteristics



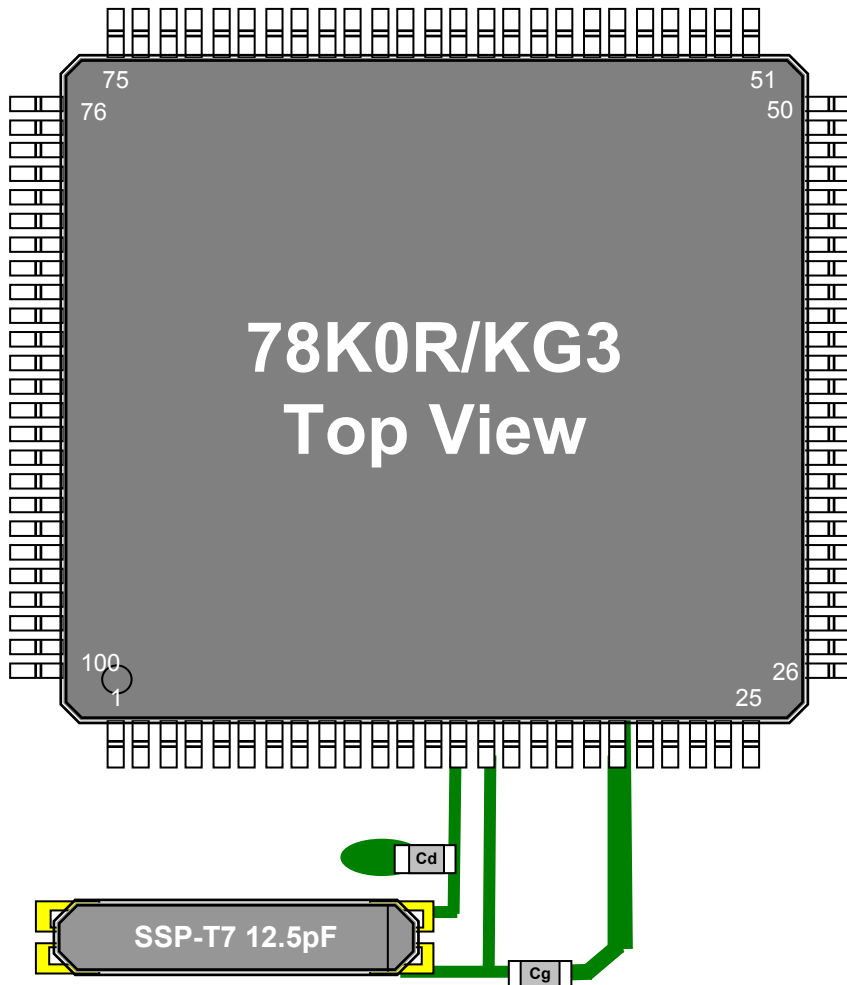
# Evaluation of Subsystem Clock Oscillation Circuit

[ $\mu$ PD78F1166GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



## Referential components layout(see Figure 1)



- Vdd:22 (H)
- Evdd:22,53(H)
- Avdd:70,73(H)
- AVss:60 (L)
- Vss:20(L)
- Evss:21,43(L)
- Avss:74(L)
- FLMD0:16(L)
- XT1:15 (SUB\_in)
- XT2:14 (SUB\_out)
- RESET:13
- REGC:19

Figure 1 Referential components layout

## Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB\_in and SUB\_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

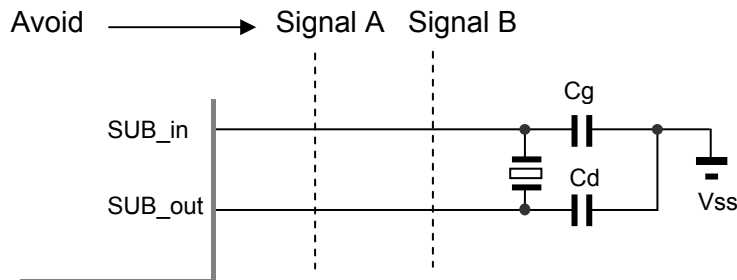


Figure 2 Example of Incorrect Board Design

**Remark** When using the subsystem clock, insert resistors  $R_d$  in series on the SUB\_out side.

# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1166GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



## [Evaluation Sample : SSP-T7 12.5pF at 25°C]

SAMPLE	No.	CL( pF )	Fo( Hz )	fr( Hz )	R1( kohm )	Co( pF )	C1( fF )	Q( k )
SSP-T7 12.5pF	1	12.5	32768.24	32765.77	41.5	0.86	2.014	58.1
	2	12.5	32768.06	32765.60	45.1	0.84	2.003	53.8
	3	12.5	32768.16	32765.70	39.8	0.85	2.004	60.9

## [IC Test Data : IC Sample Rd=0 kohm,Cg=10pF,Cd=10pF at 25°C]

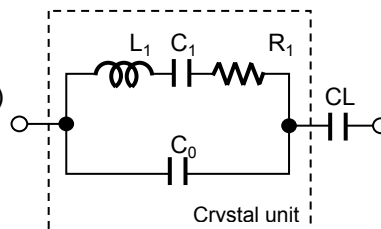
Power mode	IC Sample	Fosc( Hz )	df / f( x10 <sup>-6</sup> )	DL(x10 <sup>-6</sup> W)	-RL  ( kohm )	Vstart( V )	Ts(sec)
High	TYP	32768.30	3.05	0.26	284	1.61	1.50
	HH	32768.30	3.05	0.28	264	1.58	1.78
	HL	32768.33	3.97	0.24	314	1.59	1.36
	LH	32768.31	3.36	0.28	264	1.58	1.68
	LL	32768.34	4.27	0.24	284	1.59	1.35

## [IC Test Data : IC Sample Rd=0 kohm,Cg=10pF,Cd=10pF at 25°C]

mode	IC Sample	Fosc( Hz )	df / f( x10 <sup>-6</sup> )	DL(x10 <sup>-6</sup> W)	-RL  ( kohm )	Vstart( V )	Ts(sec)
Low	TYP	32768.21	0.24	0.13	174	1.61	1.50
	HH	32768.21	0.00	0.08	174	1.58	1.78
	HL	32768.25	1.53	0.15	204	1.59	1.36
	LH	32768.20	0.00	0.08	154	1.58	1.68
	LL	32768.25	1.53	0.15	194	1.59	1.35

### Remark ( see figure 3 )

$$F_o = f_r \times \left\{ \frac{C_1}{2 \times (C_o + C_L)} + 1 \right\} \text{ ( Hz )}$$



Fo : Load resonance frequency  
 fr : Resonance frequency  
 R1 : Motional resistance  
 C1 : Motional capacitance  
 Co : Shunt capacitance  
 CL : Load Capacitance

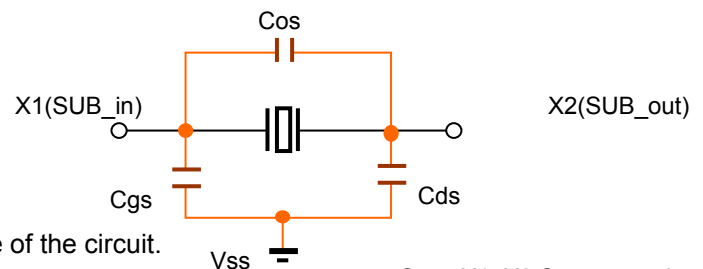
Figure 3 Equivalent circuit of crystal unit, and CL

### Remark ( see figure 4 )

Approximate formula of the load capacitance of the circuit CL.

$$CL = C_g \times C_d / (C_g + C_d) + C_s \text{ ( pF )}$$

Where Cs(=2 to 4pF) Stands for stray capacitance of the circuit.



Cos : X1\_X2 Stray capacitance  
 Cgs : X1\_Vss Stray capacitance  
 Cds : X2\_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.