

Evaluation of Subsystem Clock Oscillation Circuit

VT-200 6.0pF with S-35199A-12P[WLP(1.87x1.97)]

Measurement conditions :3.0V,1.1V

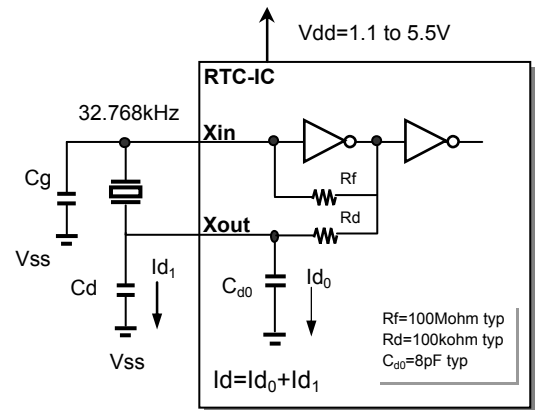
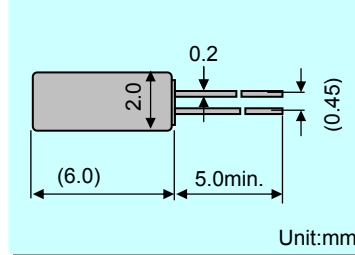


Model	:VT-200
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10 ⁶
Load capacitance	:CL=6.0pF
Equivalent series resistance	:R1=50kohm max
Max. drive level	:DL=1x10 ⁻⁶ W max
Level of drive	:DL=0.1x10 ⁻⁶ W typ

FEATURES

- 1.Compact tubular package
- 2.Photolithographic process
- 3.Excellent shock resistance and environmental characteristics.
- 4.Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)



$$CL=Cg(Cd + C_{d0}) / (Cg+Cd+C_{d0})+C_s$$

C_s, Stray capacitance

Remark) I_x : current through crystal

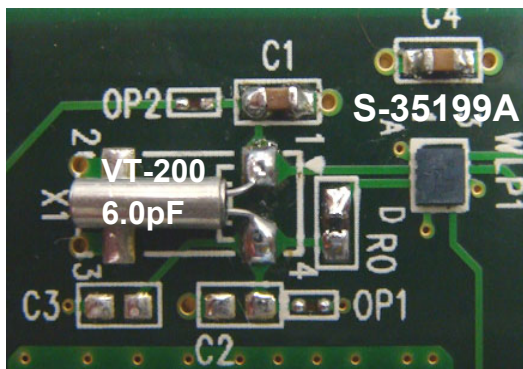
Low Consumption Power S-35x99A and VT-200 6.0pF

MODEL:VT-200 6.0pF with S-35199A at 25°C

Key specifications	Vdd=1.1V	Vdd=3.0V	Remarks
Current control resistance : Rd (k ohm)	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	3	3	Optimal capacitance in response to CL
Capacitance at drain : Cd (pF)	0	0	(CL = (Cd+C _{d0}) // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vdd=1.1V	Vdd=3.0V	Remarks
Matching Accuracy : df / f (x10 ⁻⁶)	-1.2	-1.2	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V (x10 ⁻⁶)	0.0	0.0	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL (x10 ⁻⁶ W)	0.012	0.012	DL=I _x ² Re < 1x10 ⁻⁶ W, Re=R1(1 + Co / CL) ²
Negative resistance : - RL (kohm)	857	857	5 times larger than R _{1MAX}
Oscillation allowance : M (times)	17	17	Judgemental standard of oscillation stability
Low consumption current : Id (nA)	304	304	Cd charge current, Id = ωCd*Vd < 400nA
Voltage of oscillation start : Vstart (V)	0.80	0.80	
Voltage of oscillation stop : Vstop (V)	0.49	0.49	
Oscillation start up time : Ts (sec)	0.22	0.09	Time to reach 90% of output level

Temperature characteristics of circuit		Vdd=1.1V	Vdd=3.0V	Remarks
at -40°C	Variation : df / T (x10 ⁻⁶)	-128	-128	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)
at +85°C	Variation : df / T (x10 ⁻⁶)	-137	-137	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)



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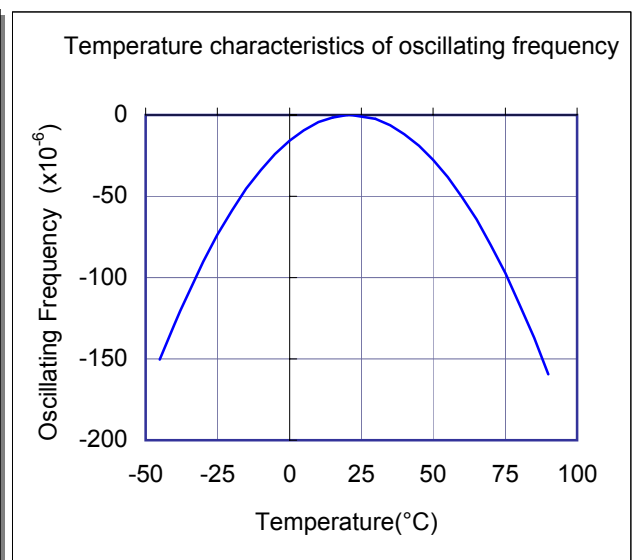
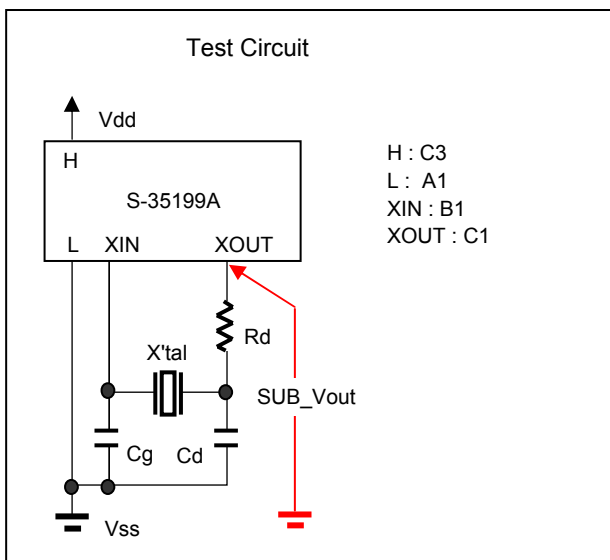
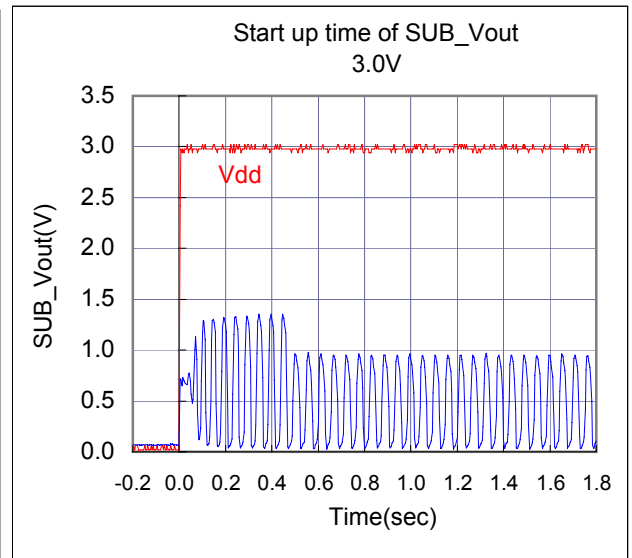
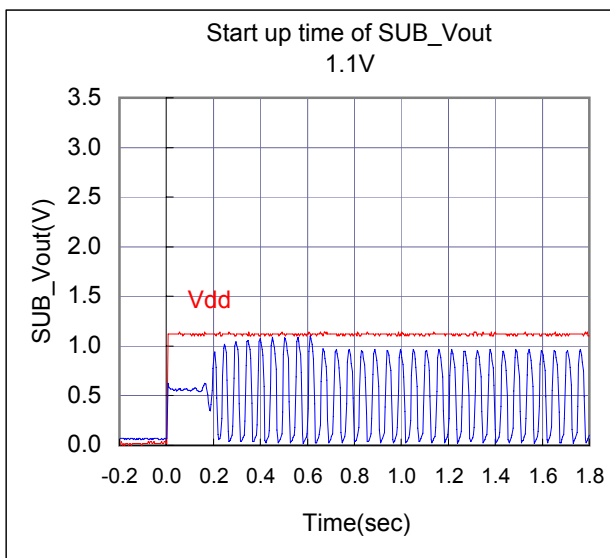
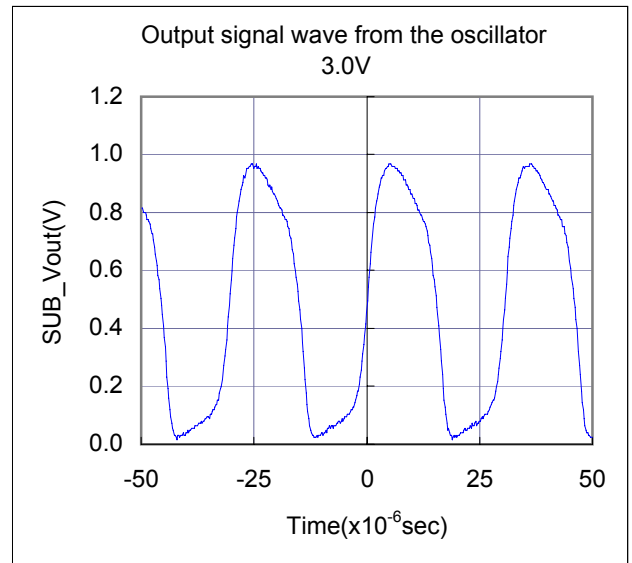
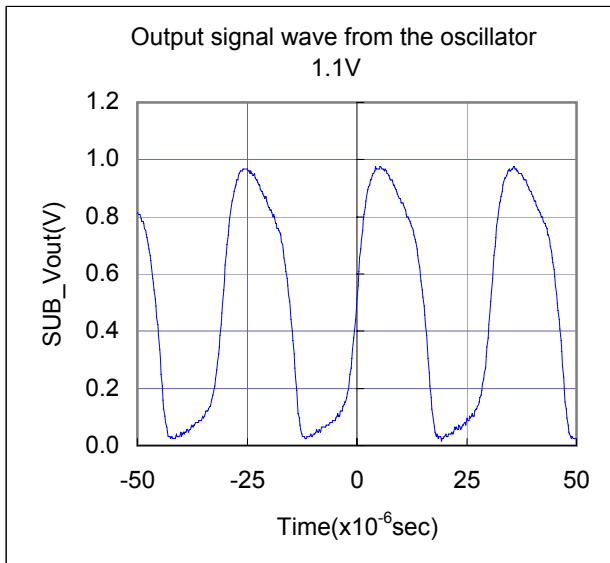
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Measurement conditions :3.0V,1.1V



Test Data at 25°C



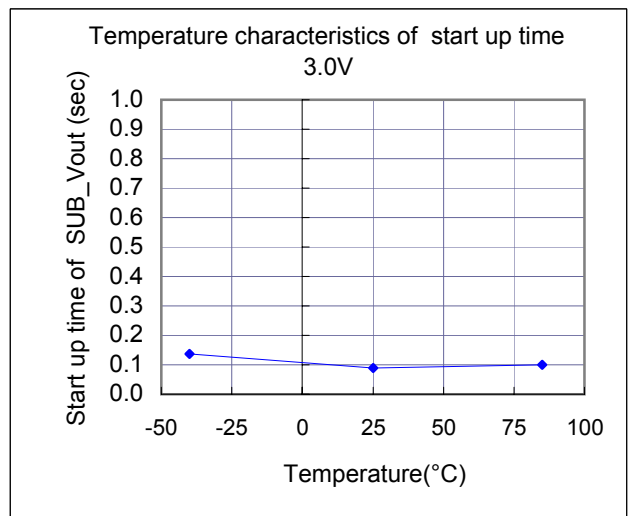
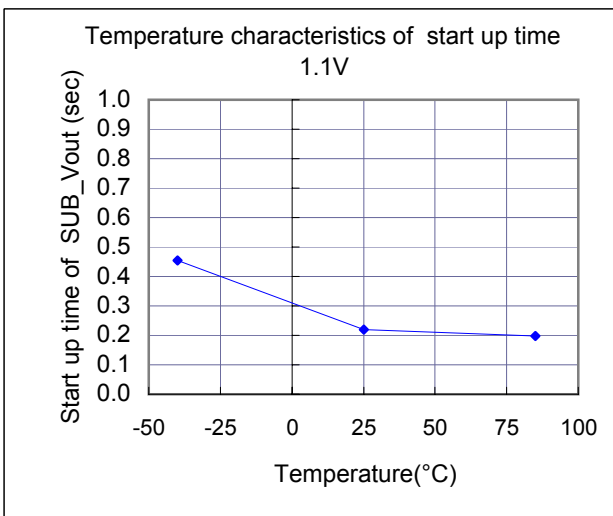
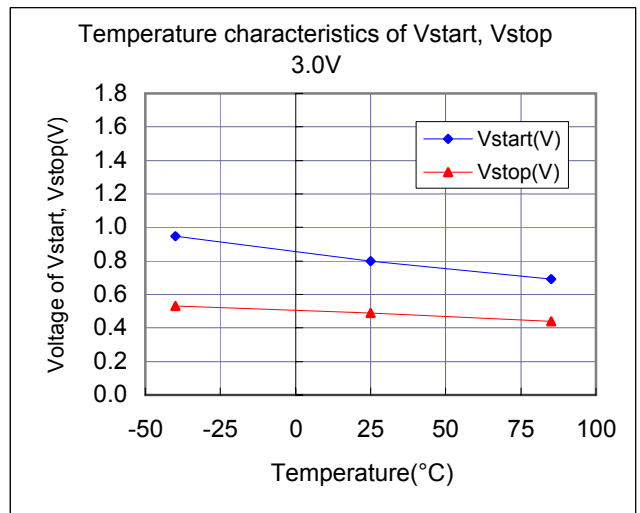
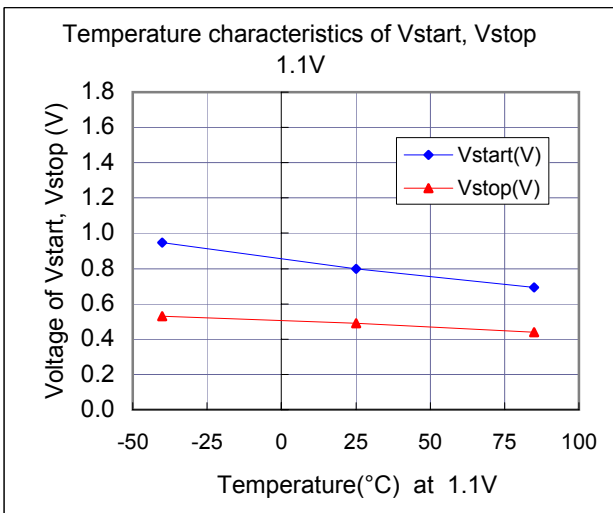
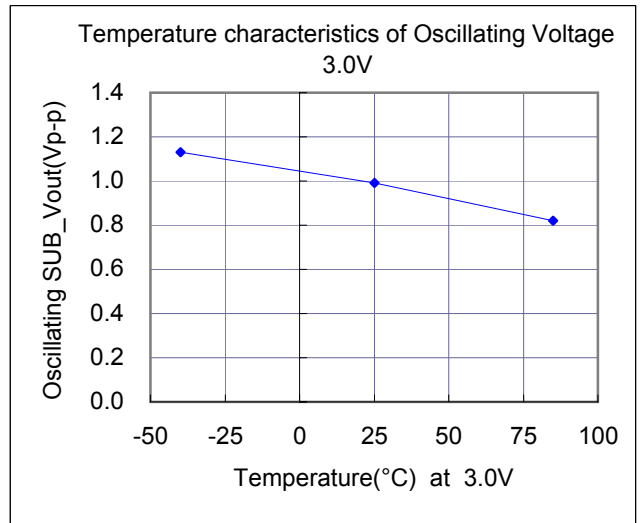
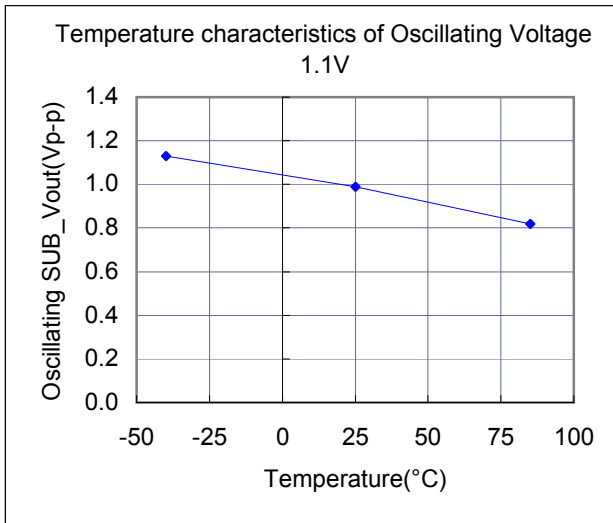
Evaluation of Subsystem Clock Oscillation Circuit

VT-200 6.0pF with S-35199A-12P[WLP(1.87x1.97)]

Measurement conditions :3.0V, 1.1V



Test Data : Temperature characteristics



The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end

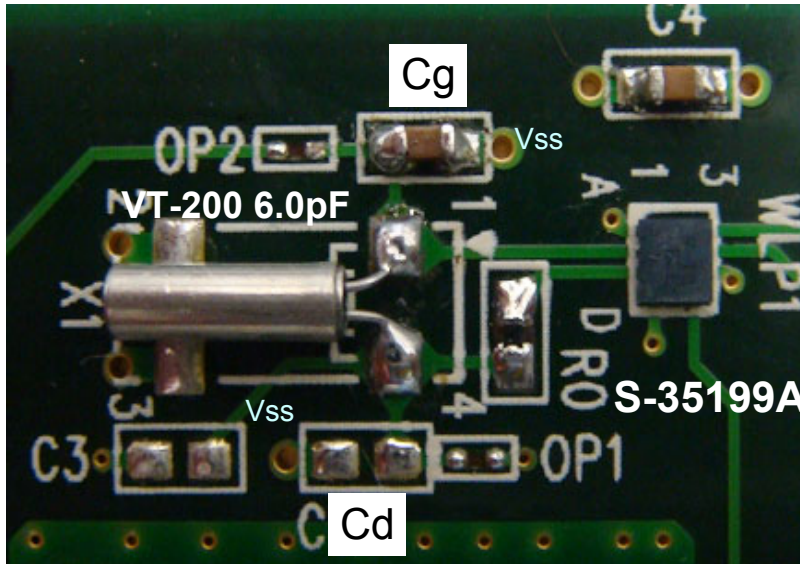
Evaluation of Subsystem Clock Oscillation Circuit

VT-200 6.0pF with S-35199A-12P[WLP(1.87x1.97)]

Measurement conditions :3.0V, 1.1V



Referential components layout(see Figure 1)



Vdd:C3(H)
 Vss: A1(L)
 X1: B1(SUB_in)
 X4: C1 (SUB_out)

Figure 1 Referential components layout

Notes for Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

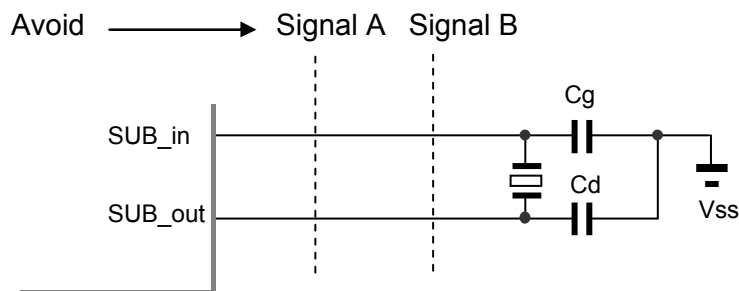


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert resistors Rd in series on the SUB_out side.

Evaluation of Subsystem Clock Oscillation Circuit

VT-200 6.0pF with S-35199A-12P[WLP(1.87x1.97)]

Measurement conditions :3.0V, 1.1V



[Evaluation Sample at 25°C]

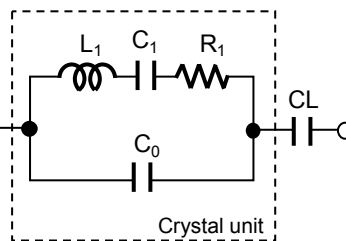
SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
VT-200 6.0pF	1	6	32768.01	32762.79	28.0	0.90	2.199	78.9
	2	6	32767.89	32762.71	27.6	0.90	2.182	80.7
	3	6	32768.10	32762.84	27.1	0.90	2.216	80.9

[IC Test Data : IC sample Rd=0 ohm,Cg=3pF,Cd=0pF at 25°C]

Vdd(V)	IC sample	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	M(times)	Id(nA)	Vstart(V)	Ts(sec)
3.0	TYP	32767.970	-1.22	0.01	857	17	304	0.80	0.09
	HH	32768.080	2.14	0.02	857	17	347	1.02	0.10
	HL	32768.028	0.55	0.01	717	14	301	0.81	0.11
	LH	32767.980	-0.92	0.01	787	16	301	0.88	0.15
	LL	32767.970	-1.22	0.01	717	14	241	0.69	0.09
1.1	TYP	32767.970	-1.22	0.01	857	17	304	0.80	0.24
	HH	32768.080	2.14	0.02	427	9	347	1.02	0.50
	HL	32768.028	0.55	0.01	717	14	301	0.81	0.29
	LH	32767.984	-0.79	0.01	857	17	301	0.88	0.40
	LL	32767.975	-1.07	0.01	717	14	241	0.69	0.21

Remark (see figure 3)

$$Fo = fr \times \{ C1 / (2 \times (Co + CL)) + 1 \} \text{ (Hz)}$$



- Fo : Load resonance frequency
- fr : Resonance frequency
- R1 : Motional resistance
- C1 : Motional capacitance
- Co : Shunt capacitance
- CL : Load Capacitance

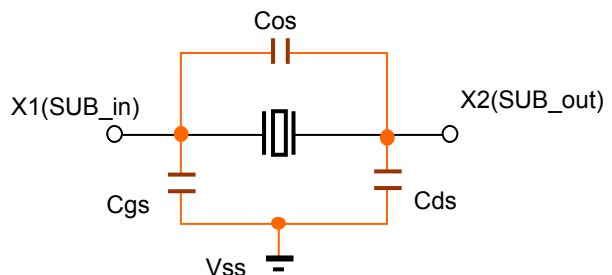
Figure 3 Equivalent circuit of crystal unit, and CL

Remark (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

$$CL = Cg \times Cd / (Cg + Cd) + Cs \text{ (pF)}$$

Where Cs Stands for stray capacitance of the circuit.



- Cos : X1_X2 Stray capacitance
- Cgs : X1_Vss Stray capacitance
- Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

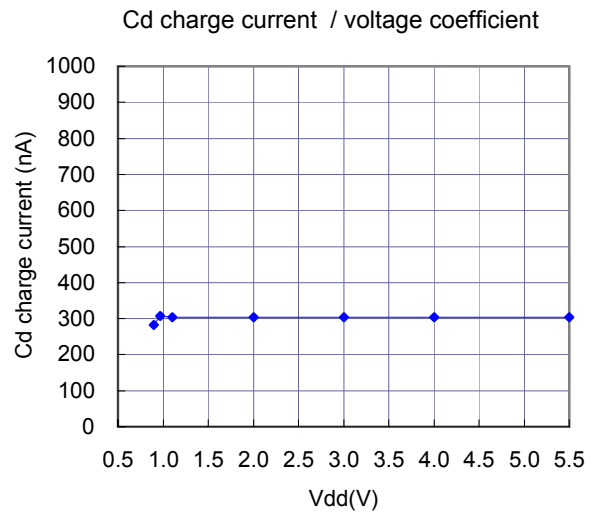
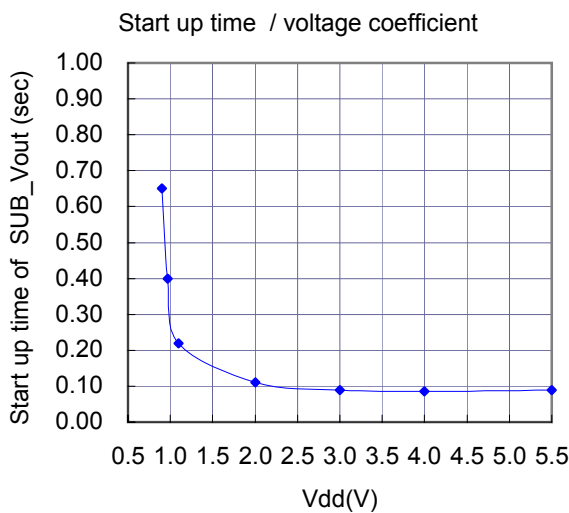
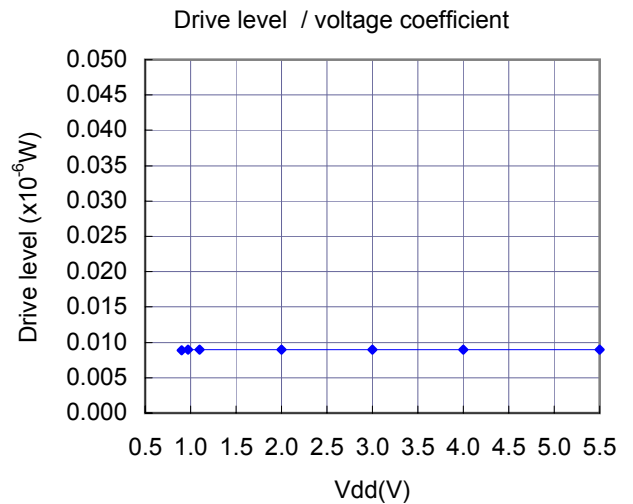
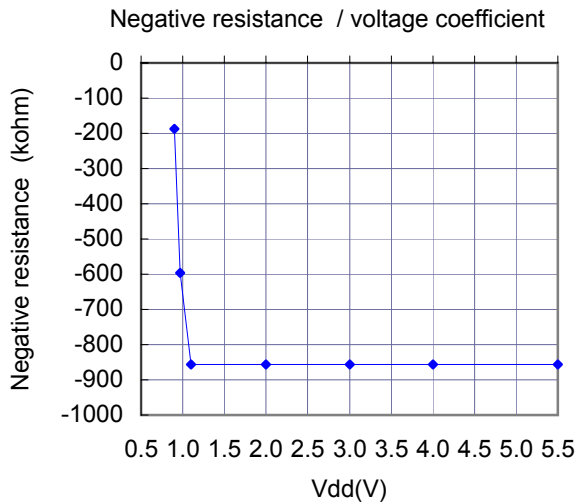
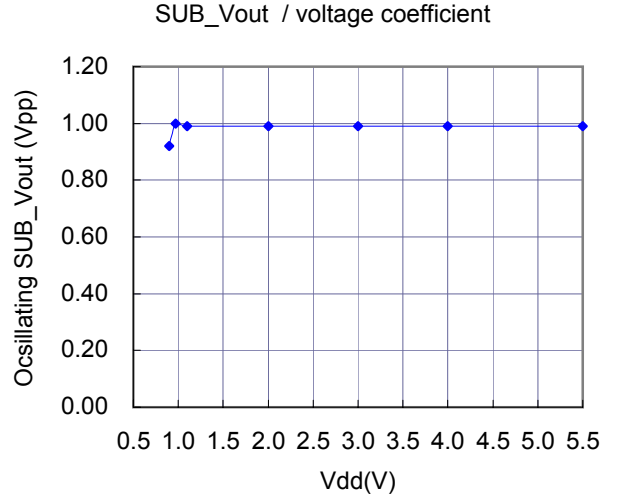
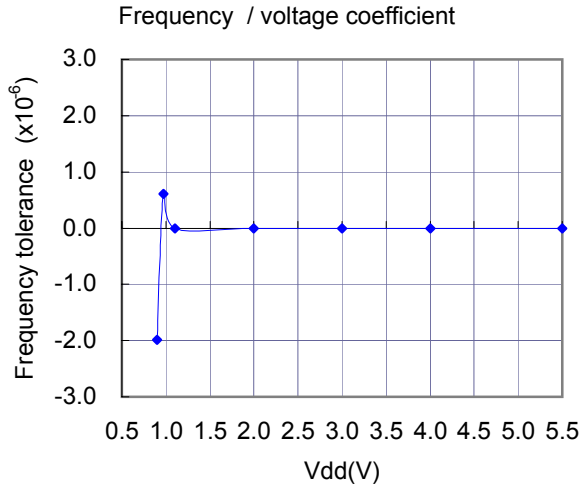
Evaluation of Subsystem Clock Oscillation Circuit

VT-200 6.0pF with S-35199A-12P[WLP(1.87x1.97)]

Measurement conditions : Vdd=(0.9V) to 5.5V at 25°C



Referential Data(1) : Voltage characteristics



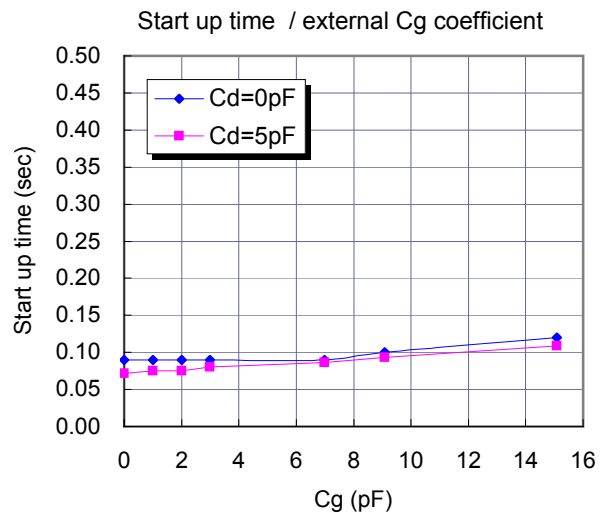
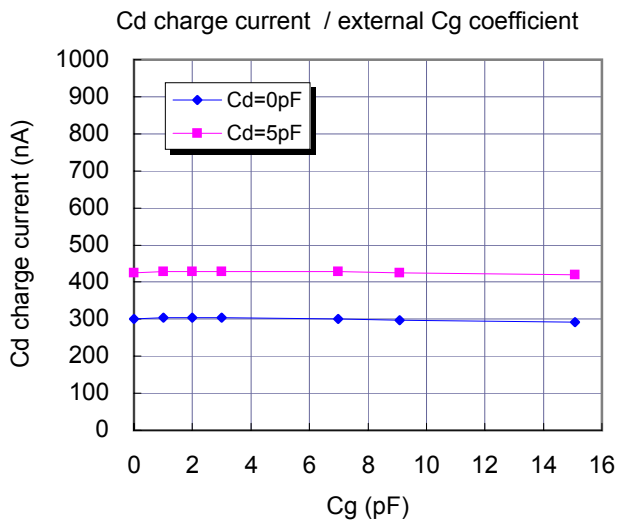
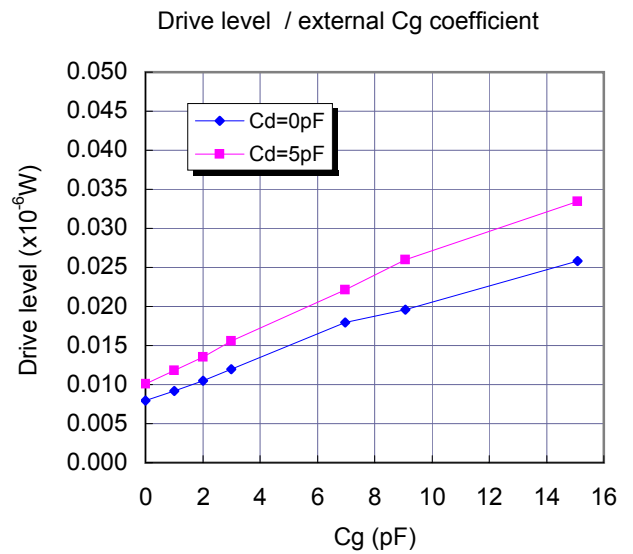
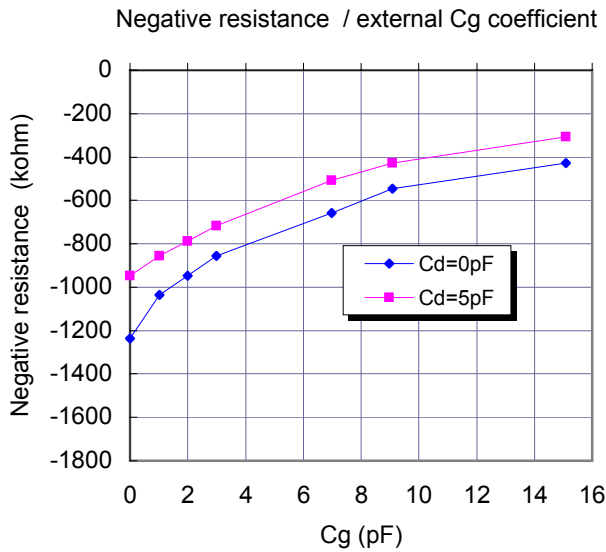
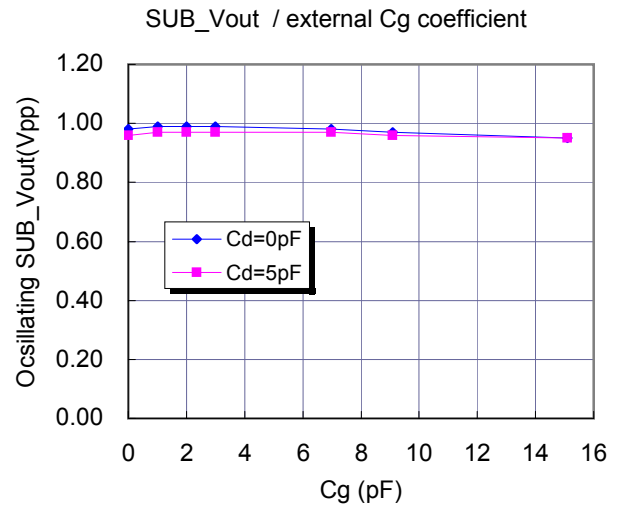
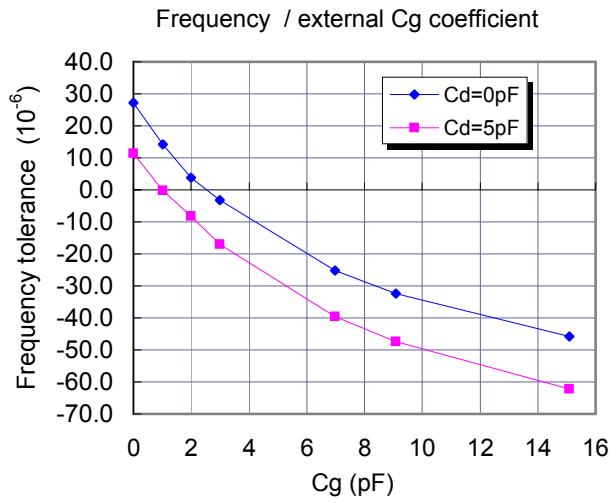
Evaluation of Subsystem Clock Oscillation Circuit

VT-200 6.0pF with S-35199A-12P[WLP(1.87x1.97)]

Measurement conditions : Vdd=3.0V at 25°C



Referential Data(2) : External capacitance Cg characteristics



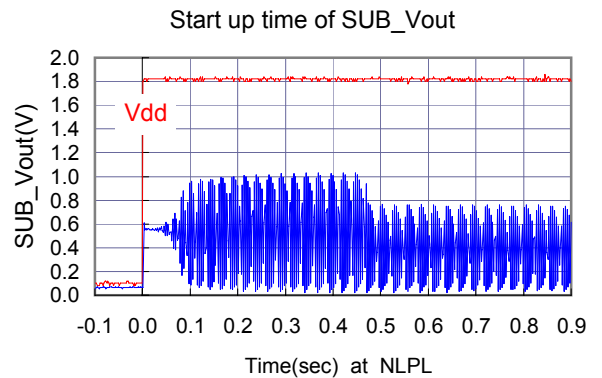
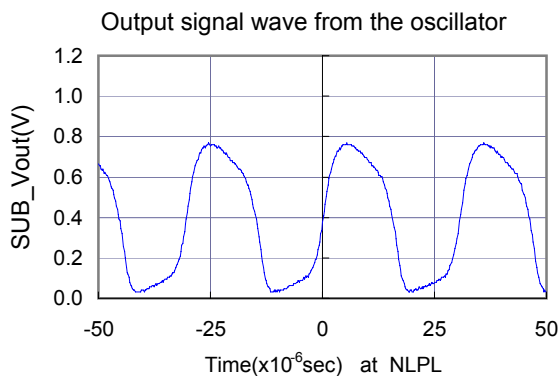
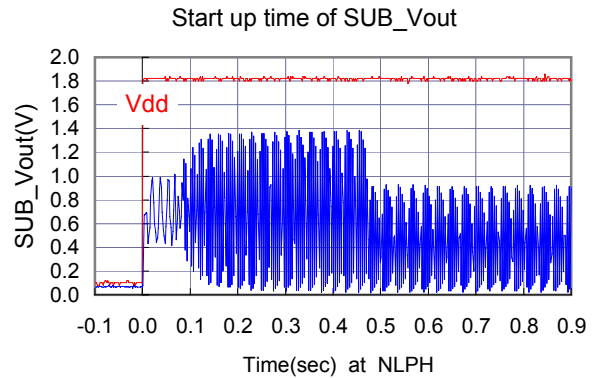
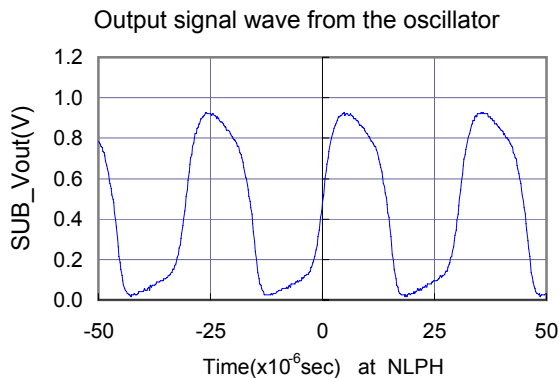
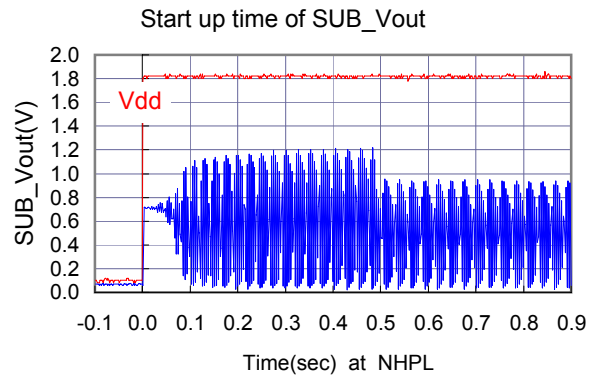
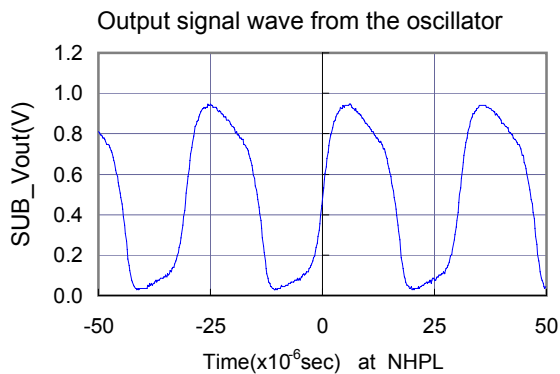
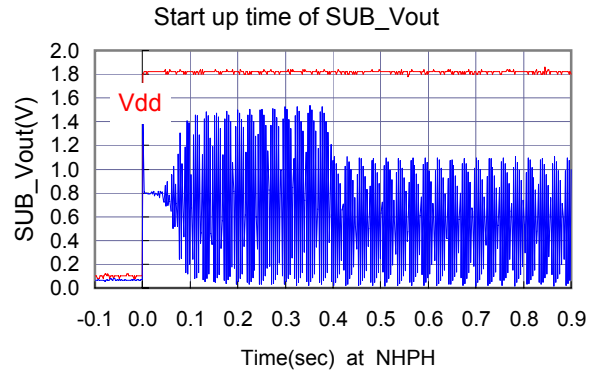
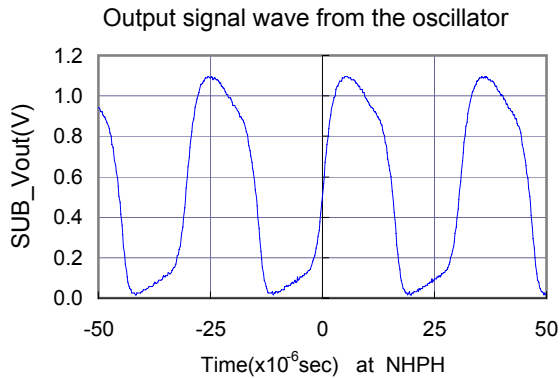
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VT-200 6.0pF with S-35199A-12P[WLP(1.87x1.97)]

Measurement conditions : Vdd=1.8V at 25°C



Referential Data(3) : RTC sample(NHPH,NHPL,NLPH,NLPL)



Evaluation of Subsystem Clock Oscillation Circuit

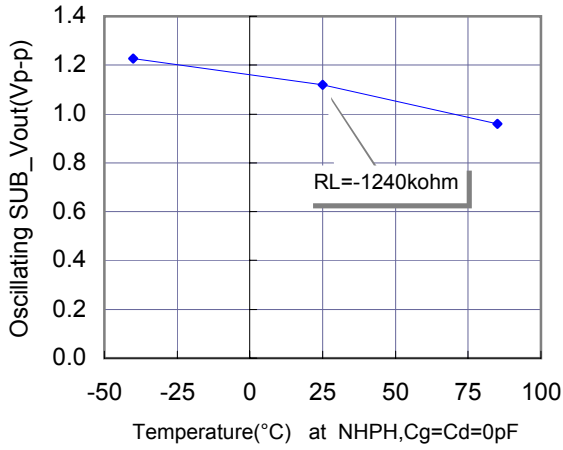
VT-200 6.0pF with S-35199A-12P[WLP(1.87x1.97)]

Measurement conditions : Vdd=3.0V at -40°C to 85°C

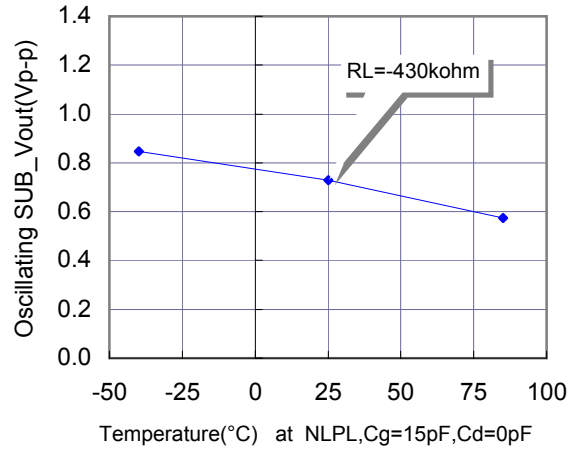


Referential Data(4) : Temperature characteristics (NHPH,NLPL)

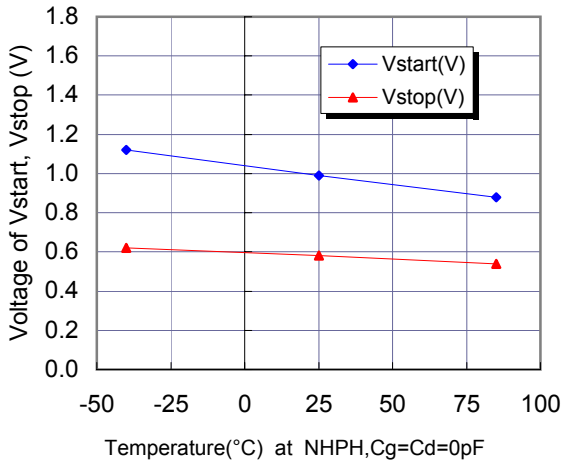
Temperature characteristics of Oscillating Voltage



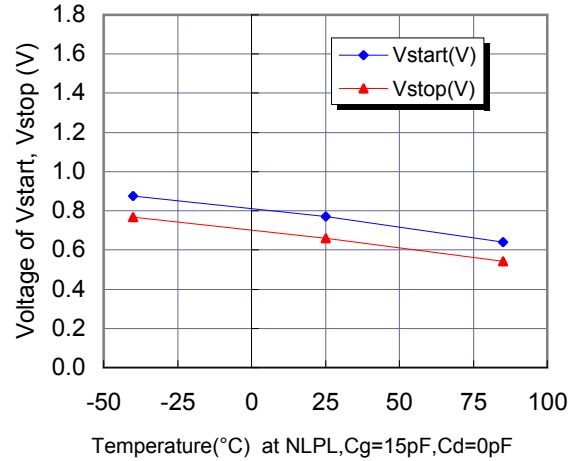
Temperature characteristics of Oscillating Voltage



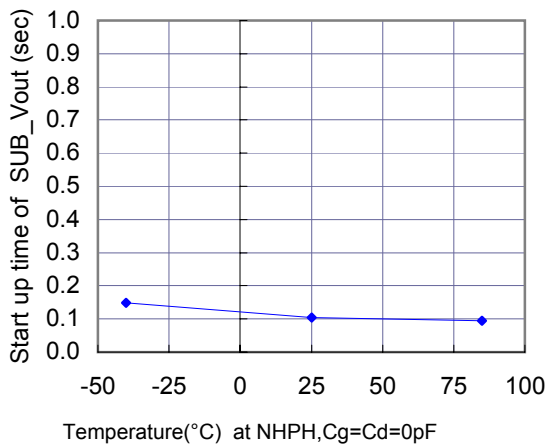
Temperature characteristics of Vstart, Vstop



Temperature characteristics of Vstart, Vstop



Temperature characteristics of start up time



Temperature characteristics of start up time

