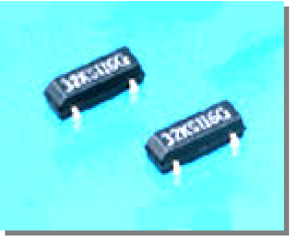
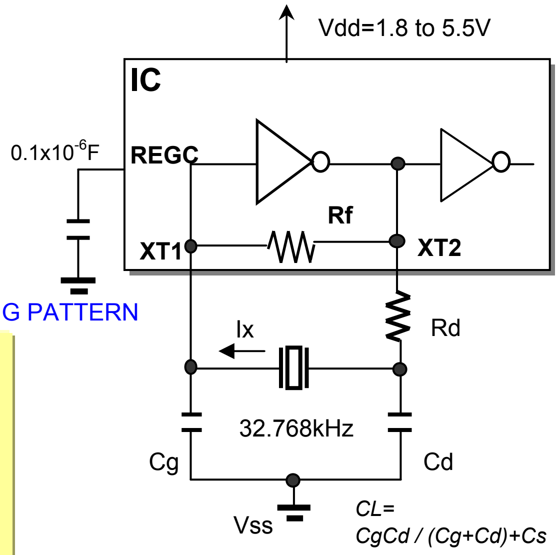
# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F1166GC-16BT] QFP(14x14) 0.50mm pitch

Measurement conditions : 5.0V



| | |
|---|---|
| Model | :SP-T2A |
| Frequency | :Fo=32.768kHz |
| Frequency tolerance | :dF/Fo= +/-20x10$^{-6}$ |
| Load capacitance | :CL=12.5pF |
| Equivalent series resistance | :R1=50k ohm max |
| Max. Drive level | :DL=1x10$^{-6}$W max |
| Recommended drive level | :DL=0.1x10$^{-6}$W typ |

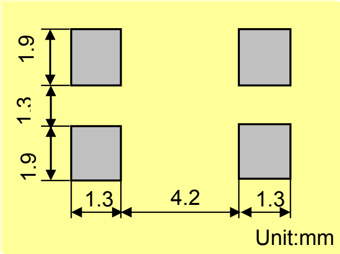



*Remark) Ix : current through crystal*

## FEATURES

1. Plastic mold package incorporated tubular type quartz crystal.
2. Suitable for automatic and high density surface mounting.
3. Excellent shock and heat resistance
4. Real time clocks, Timers, Portable applications,Clock source for Micro-Computers

## RECOMMENDED SOLDERING PATTERN




MODEL:SP-T2A 12.5pF with uPD78F1166GC at 25°C

| Key specifications | Low | High | Remarks |
|---|---|---|---|
| Current control resistance : Rd ( k ohm ) | 0 | 0 | Control drive level & secure phase margin |
| Capacitance at gate : Cg ( pF ) | 10 | 12 | Optimal capacity in response to CL |
| Capacitance at drain : Cd ( pF ) | 10 | 12 | ( CL = Cd // Cg + stray capacitance ) |

| Circuit characteristics ( at 25°C ) | Low | High | Remarks |
|---|---|---|---|
| Matching Accuracy : df / f ( x10$^{-6}$ ) | 2.4 | -0.2 | Frequency offset volume at specified Vdd |
| Voltage Fluctuation : +/-df / V ( x10$^{-6}$ ) | 0.0 | 0.0 | Vdd +/-10% ( Standard operating voltage range ) |
| Drive Level : DL ( x10$^{-6}$W ) | 0.13 | 0.31 | DL=Ix$^2$ Re < 1x10$^{-6}$W,Re=R1( 1 + Co / CL )$^2$ |
| Negative resistance : \| - RL \| ( kohm ) | 171 | 281 | 5 times larger than $R_{1MAX}$ |
| Oscillation allowance : M ( times ) | 3.4 | 5.6 | Judgemental standard of oscillation stability |
| Voltage of oscillation start : Vstart (V ) | 1.60 | 1.60 | |
| Voltage of oscillation stop : Vstop (V ) | 1.59 | 1.59 | |
| Oscillation start up time : Ts ( sec ) | 1.39 | 1.37 | Time to reach 90% of output level |

| Temperature characteristics of circuit | | Low | High | Remarks |
|---|---|---|---|---|
| at -40°C | Variation : df / T ( x10$^{-6}$ ) | -130 | -129 | Typ.Tp=25°C ( K = -3.5×10$^{-8}$ / °C$^2$ ) |
| at +85°C | Variation : df / T ( x10$^{-6}$ ) | -132 | -132 | Typ.Tp=25°C ( K = -3.5×10$^{-8}$ / °C$^2$ ) |

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarante the product's characteristics. Please review and check above parameters at customer's end.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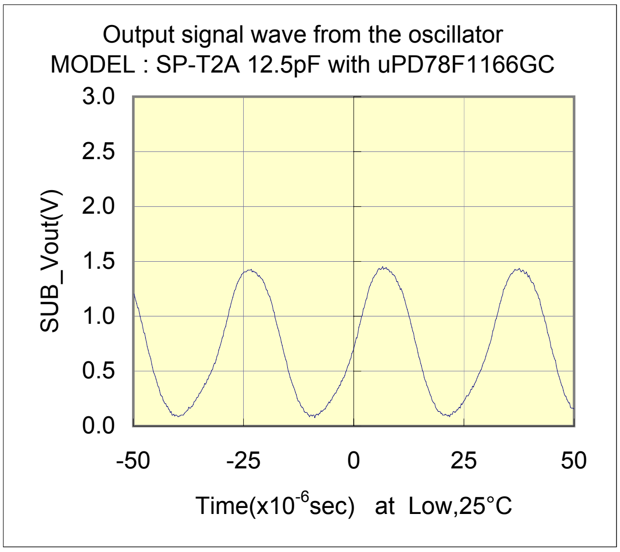
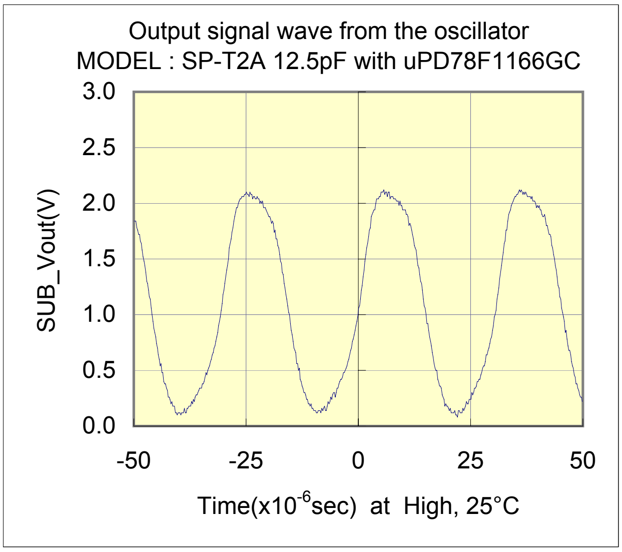
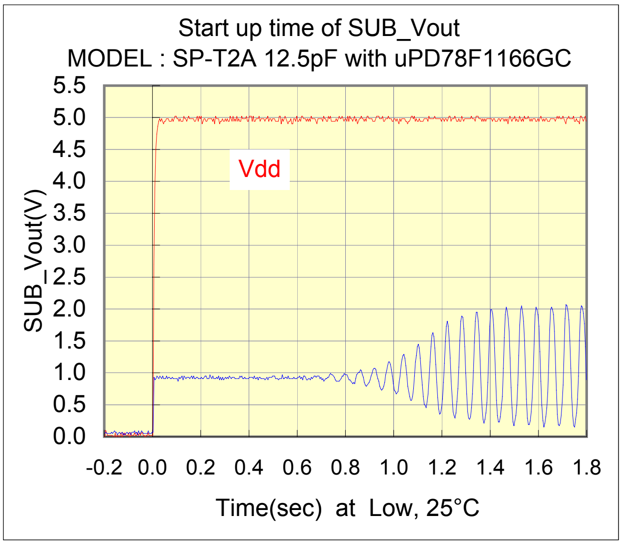
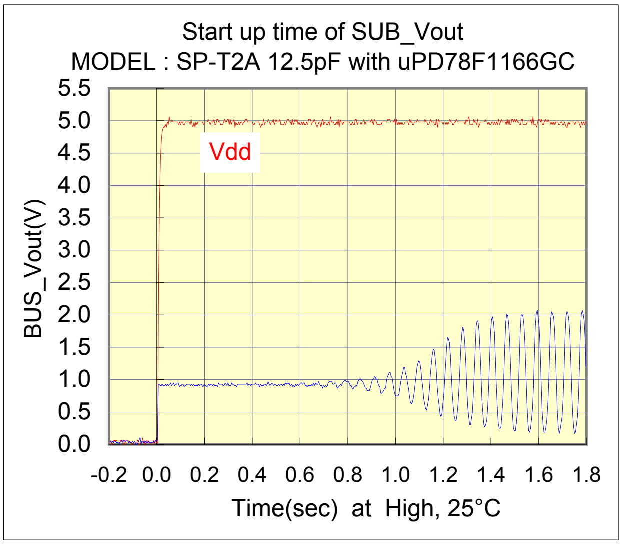
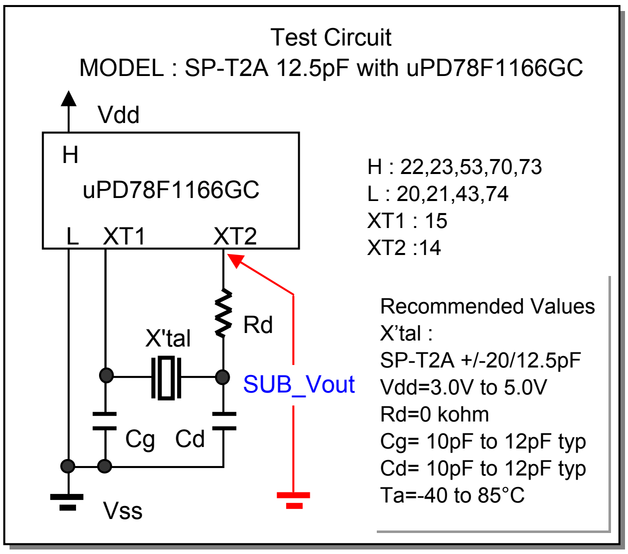
## Test Data

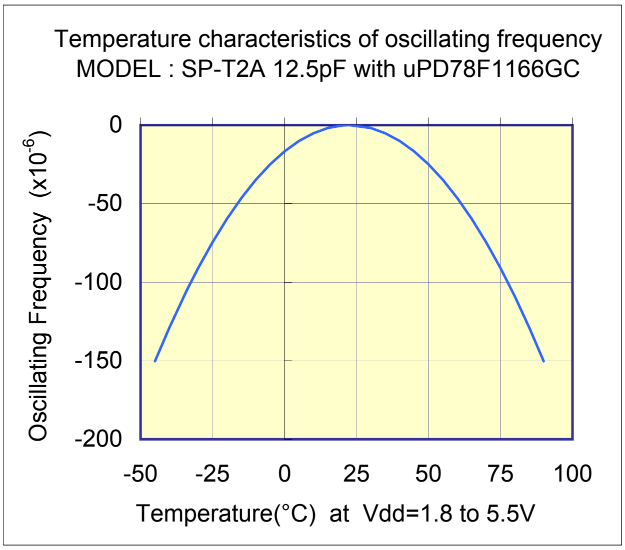


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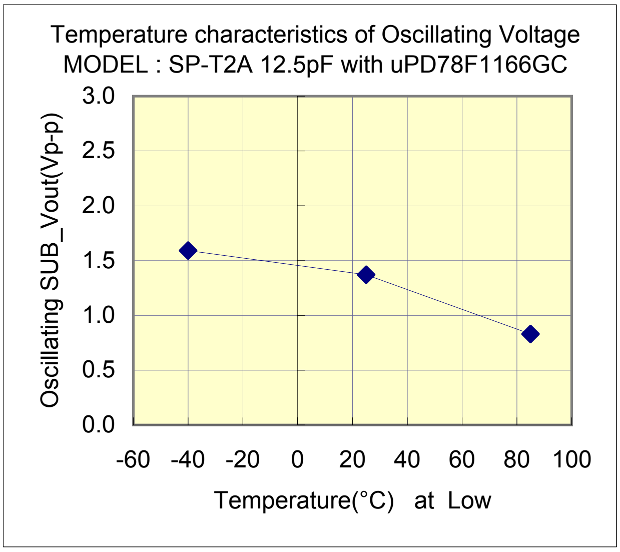
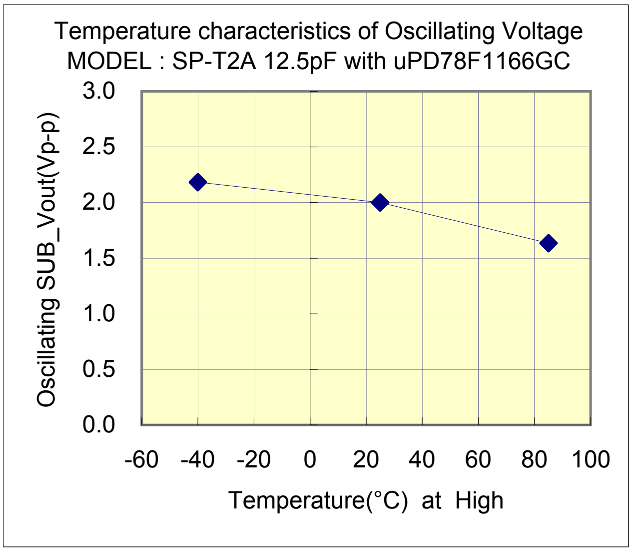
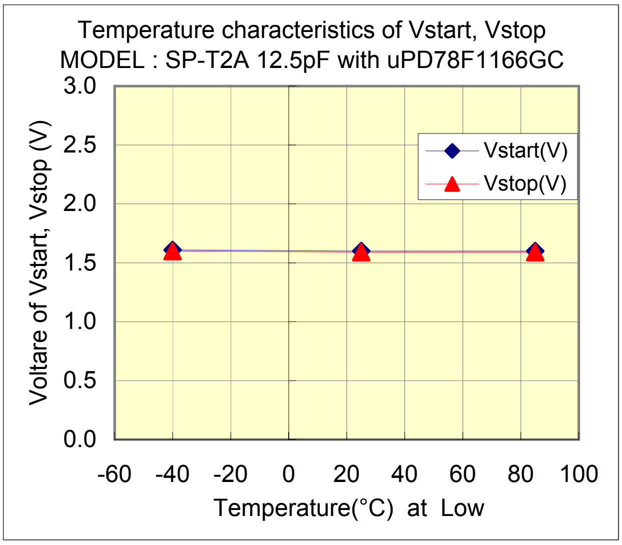
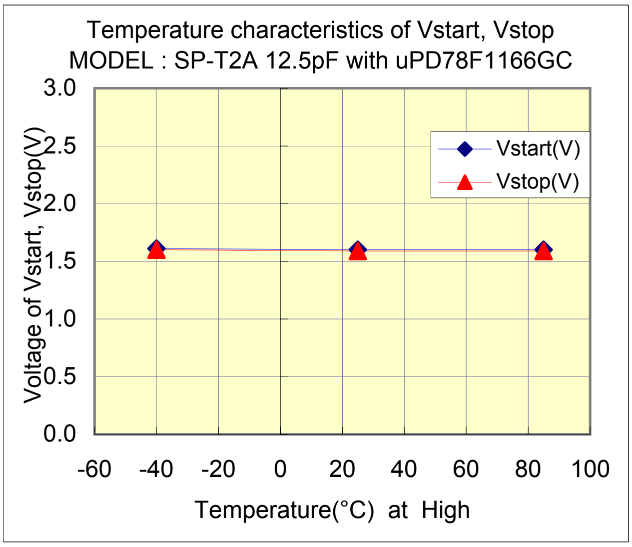
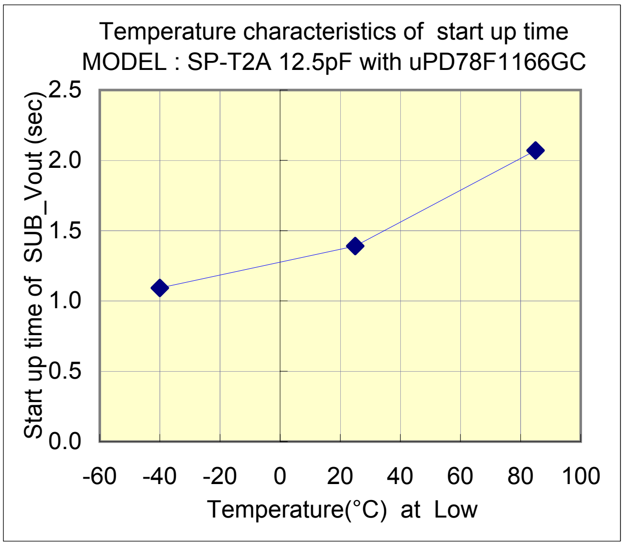
## Test Data : Temperature characteristics

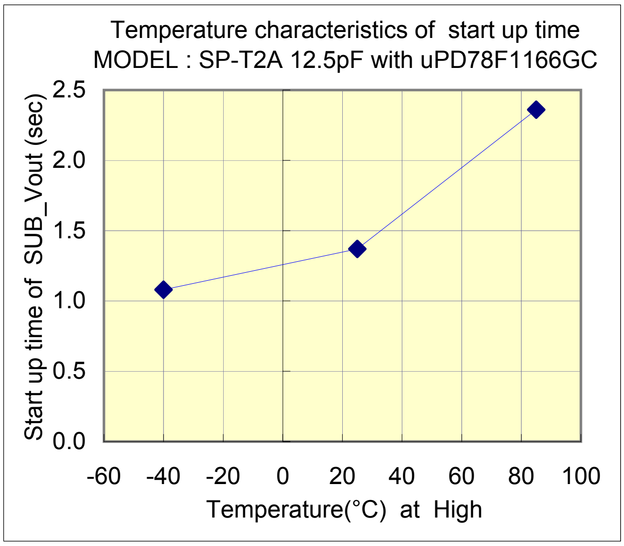


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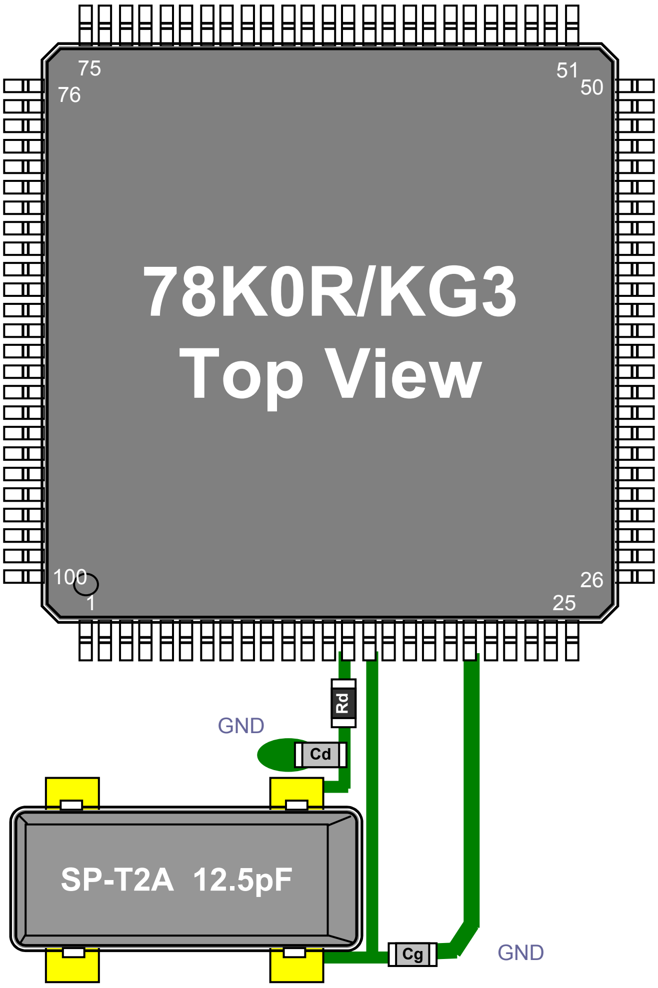
**Referential components layout(see Figure 1)**




Vdd:22 (H)
Evdd:22,53(H)
Avdd:70,73(H)
AVss:60 (L)
Vss:20(L)
Evss:21,43(L)
Avss:74(L)
FLMD0:16(L)
XT1:15 (SUB_in)
XT2:14 (SUB_out)
RESET:13
REGC:19

**Figure 1 Referential components layout**

**Notes Board Design**

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.
Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

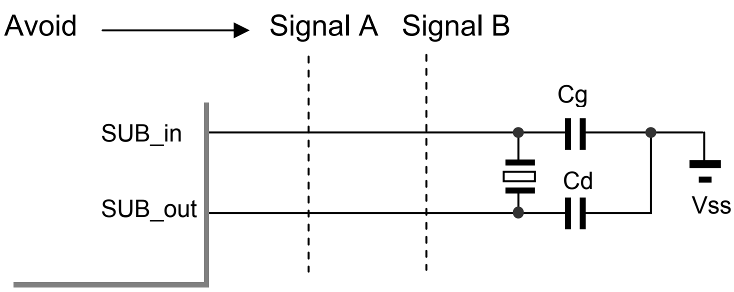



**Figure 2 Example of Incorrect Board Design**

**Remark** When using the subsystem clock, insert resistors Rd in series on the SUB_out side.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## [Evaluation Sample : SP-T2A 12.5pF at 25°C]

| SAMPLE | No. | CL( pF ) | Fo( Hz ) | fr( Hz ) | R1( kohm ) | Co( pF ) | C1( fF ) | Q( k ) |
|---|---|---|---|---|---|---|---|---|
| SP-T2A 12.5pF | 1 | 12.5 | 32768.02 | 32765.27 | 34.8 | 1.05 | 2.275 | 61.4 |
| | 2 | 12.5 | 32768.06 | 32765.34 | 36.9 | 1.02 | 2.245 | 58.7 |
| | 3 | 12.5 | 32768.13 | 32765.43 | 36.9 | 1.01 | 2.227 | 59.2 |

## [IC Test Data : IC Sample Rd=0 kohm,Cg=12pF,Cd=12pF at 25°C]

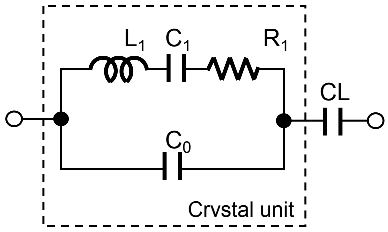
| mode | IC Sample | Fosc( Hz ) | df / f( $x10^{-6}$ ) | DL($x10^{-6}$W) | \| -RL \|( kohm ) | Vstart( V ) | Ts(sec) |
|---|---|---|---|---|---|---|---|
| High | TYP | 32768.02 | -0.15 | 0.31 | 281 | 1.60 | 1.37 |
| | HH | 32768.01 | -0.31 | 0.32 | 261 | 1.60 | 1.87 |
| | HL | 32768.04 | 0.61 | 0.29 | 311 | 1.59 | 1.33 |
| | LH | 32768.01 | -0.31 | 0.32 | 261 | 1.57 | 1.75 |
| | LL | 32768.04 | 0.61 | 0.29 | 311 | 1.58 | 1.35 |

## [IC Test Data : IC Sample Rd=0 kohm,Cg=10pF,Cd=10pF at 25°C]

| mode | IC Sample | Fosc( Hz ) | df / f( $x10^{-6}$ ) | DL($x10^{-6}$W) | \| -RL \|( kohm ) | Vstart( V ) | Ts(sec) |
|---|---|---|---|---|---|---|---|
| Low | TYP | 32768.10 | 2.44 | 0.13 | 171 | 1.60 | 1.39 |
| | HH | 32768.10 | 1.68 | 0.07 | 151 | 1.59 | 1.68 |
| | HL | 32768.12 | 3.05 | 0.14 | 201 | 1.59 | 1.28 |
| | LH | 32768.08 | 1.83 | 0.08 | 151 | 1.59 | 1.63 |
| | LL | 32768.13 | 3.36 | 0.14 | 201 | 1.59 | 1.27 |

**Remark ( see figure 3 )**

Fo = fr ×{ C1/ ( 2×( Co + CL ) + 1 } ( Hz )




Fo : Load resonance frequency
fr : Resonance frequency
R1 : Motional resistance
C1 : Motional capacitance
Co : Shunt capacitance
CL : Load Capacitance

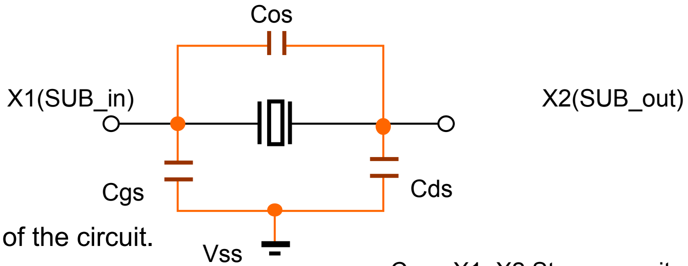
**Figure 3 Equivalent circuit of crystal unit, and CL**

**Remark ( see figure 4)**

Approximate formula of the load capacitance of the circuit CL.

CL = Cg×Cd / (Cg + Cd) + Cs (pF)

Where Cs(=2 to 4pF) Stands for stray capacitance of the circuit.




Cos : X1_X2 Stray capacitance
Cgs : X1_Vss Stray capacitance
Cds : X2_Vss Stray capacitance

**Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit**

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.