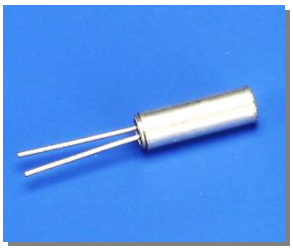
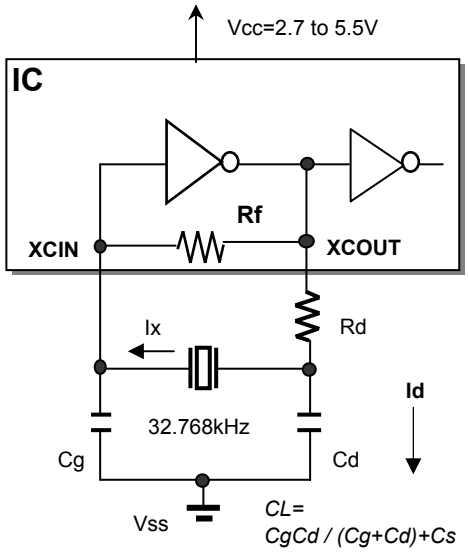
Evaluation of Subsystem Clock Oscillation Circuit

VT-200 12.5pF with R4F20103NFB-64P [LQFP(14x14) 0.80mm pitch]

Measurement conditions : 3.3V ,5.0V



Model	:VT-200
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10^{-6}
Load capacitance	:CL=12.5pF
Equivalent series resistance	:R1=50kohm max
Max. drive level	:DL=1x10^{-6}W max
Level of drivel	:DL=0.1x10^{-6}W typ

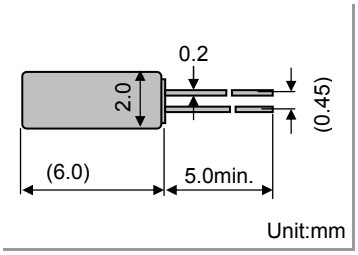


Remark) Ix : current through crystal

FEATURES

1.Compact tubular package
2.Photolithographic process
3.Excellent shock resistance and environmental characteristics.
4.Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)



MODEL:VT-200 12.5pF with R4F20103NFB at 25°C

Key specifications	Vcc=3.3V	Vcc=5.0V	Remarks
Current control resistance : Rd (k ohm)	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	22	22	Optimal capacitance in response to CL
Capacitance at drain : Cd (pF)	22	22	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vcc=3.3V	Vcc=5.0V	Remarks
Matching Accuracy : df / f (x10^{-6})	-1.8	-1.5	Frequency offset volume at specified Vcc
Voltage Fluctuation : +/-df / V (x10^{-6})	0.1	0.1	Vcc +/-10% (Standard operating voltage range)
Drive Level : DL (x10^{-6}W)	0.09	0.09	DL=Ix^2 Re < 1x10^{-6}W,Re=R1(1 + Co / CL)^2
Negative resistance : | - RL | (kohm)	1134	1234	5 times larger than R_{1MAX}
Oscillation allowance : M (times)	23	25	Judgemental standard of oscillation stability
Normal consumption current : Id (nA)	1,021	1,021	Cd charge current, Id = ωCd*Vd
Voltage of oscillation start : Vstart (V)	1.05	1.05	
Voltage of oscillation stop : Vstop (V)	0.89	0.89	
Oscillation start up time : Ts (sec)	0.49	0.49	Time to reach 90% of output level

Temperature characteristics of circuit		Vcc=3.3V	Vcc=5.0V	Remarks
at -40°C	Variation : df / T (x10^{-6})	-139	-139	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^2)
at +85°C	Variation : df / T (x10^{-6})	-126	-126	Typ.Tp=25°C (K = -3.5×10^{-8} / °C^2)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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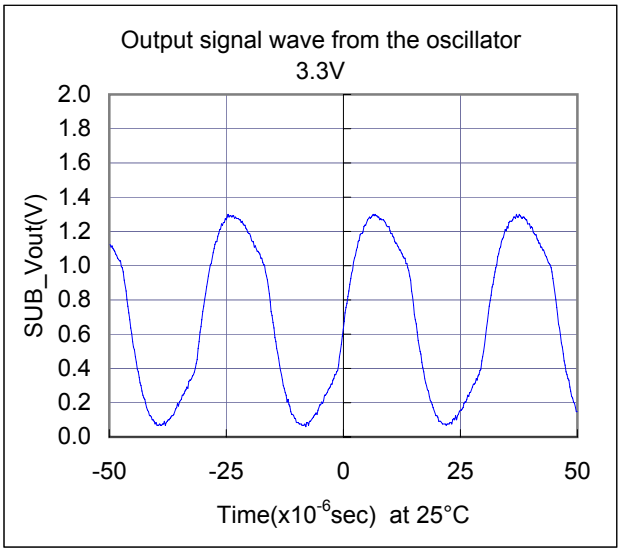
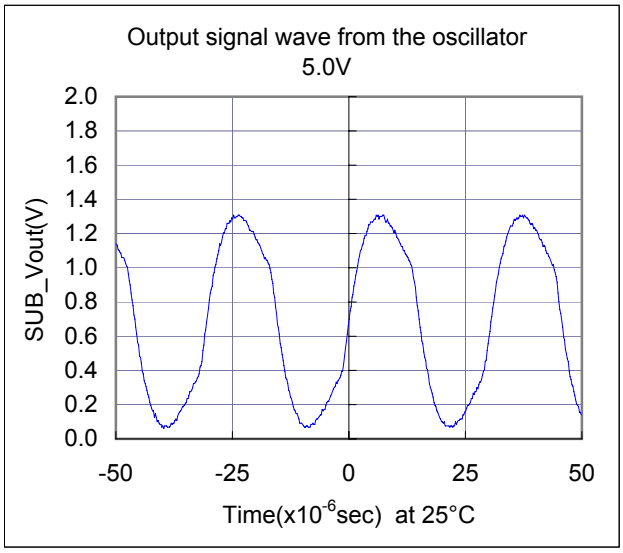
Evaluation of Subsystem Clock Oscillation Circuit

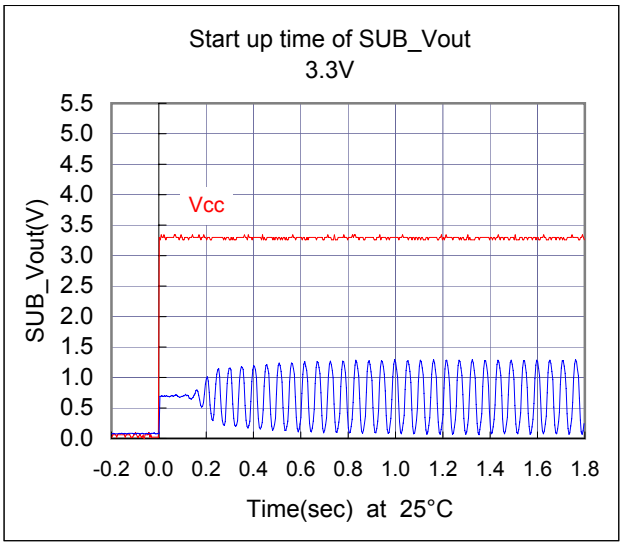
VT-200 12.5pF with R4F20103NFB-64P [LQFP(14x14) 0.80mm pitch]

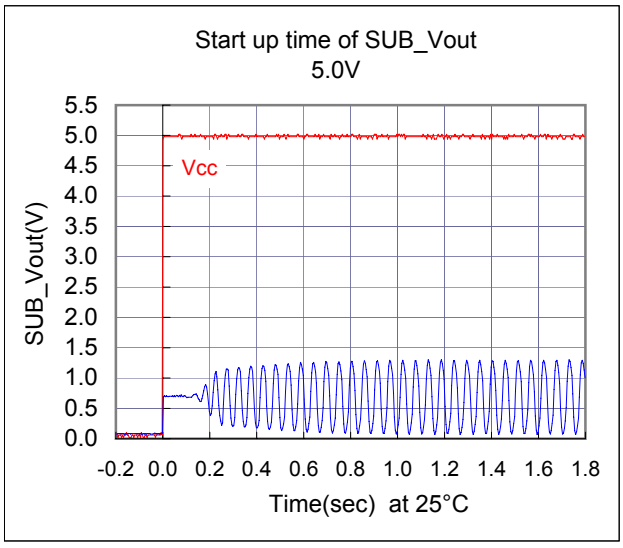
Measurement conditions : 3.3V ,5.0V

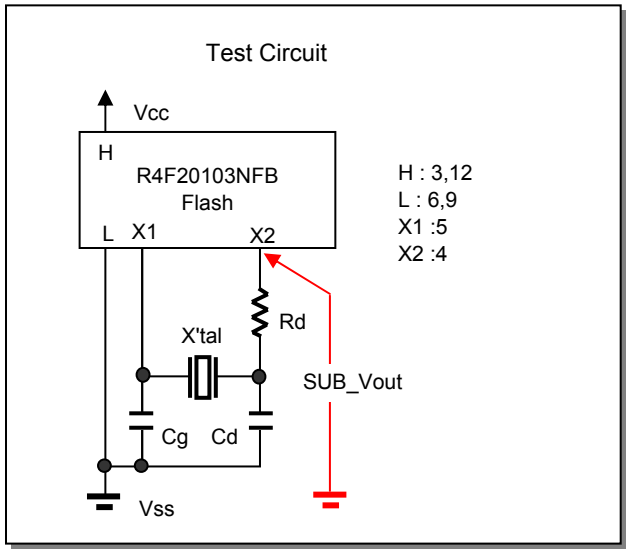
Test Data

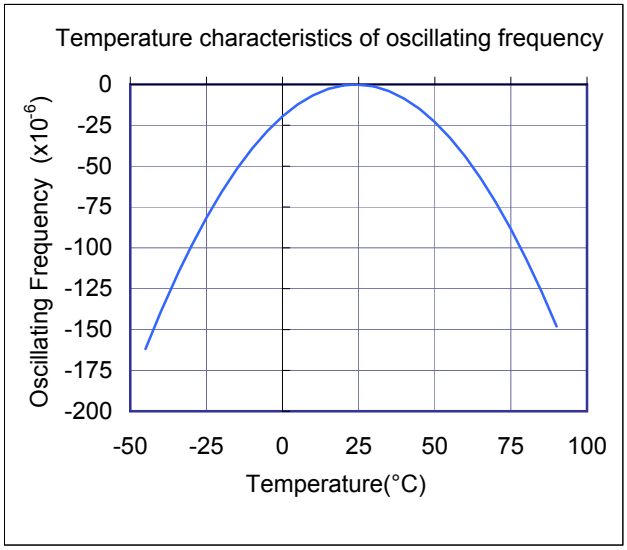












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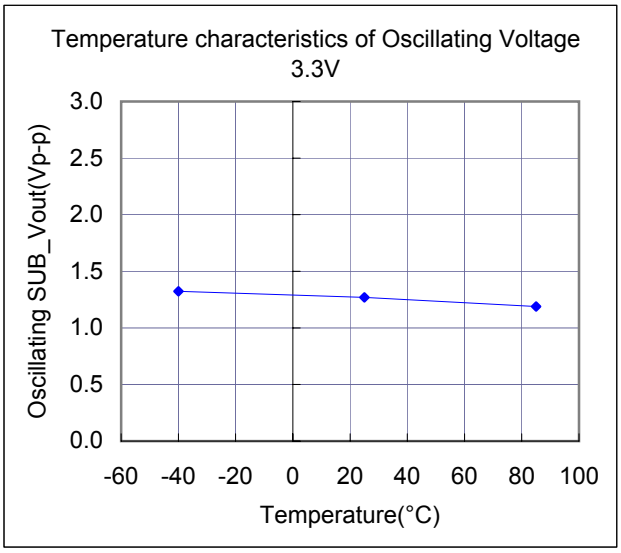
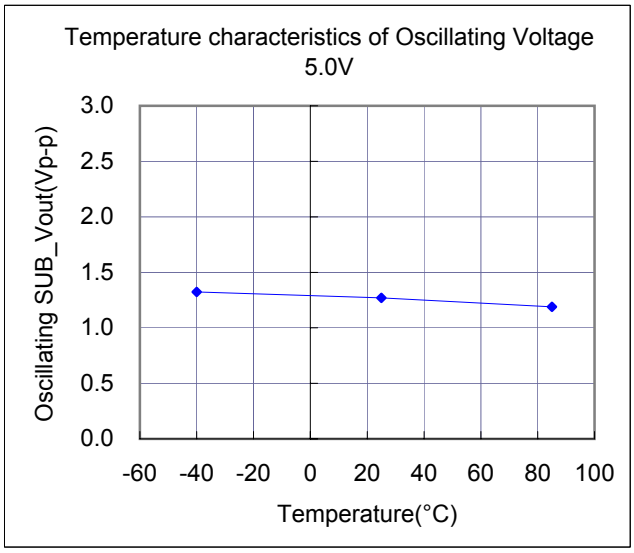
Evaluation of Subsystem Clock Oscillation Circuit

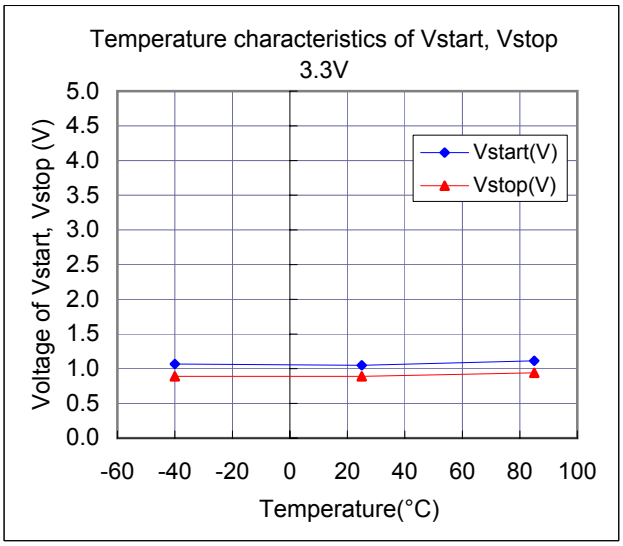
VT-200 12.5pF with R4F20103NFB-64P [LQFP(14x14) 0.80mm pitch]

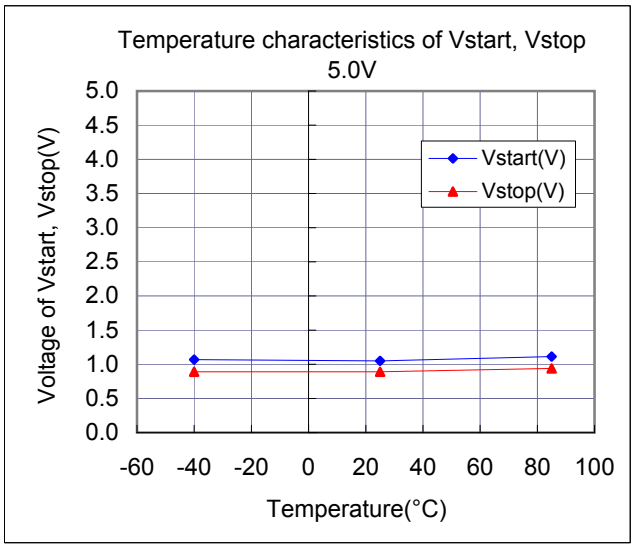
Measurement conditions : 3.3V ,5.0V

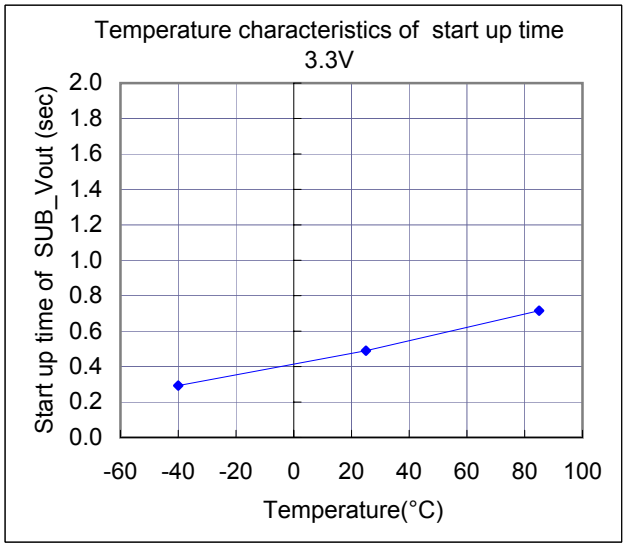
Test Data : Temperature characteristics

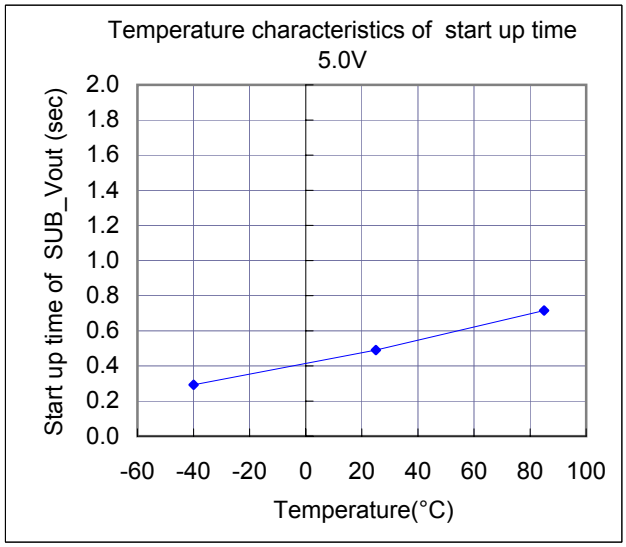












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Evaluation of Subsystem Clock Oscillation Circuit

VT-200 12.5pF with R4F20103NFB-64P [LQFP(14x14) 0.80mm pitch]

Measurement conditions : 3.3V ,5.0V

Referential components layout(see Figure 1)

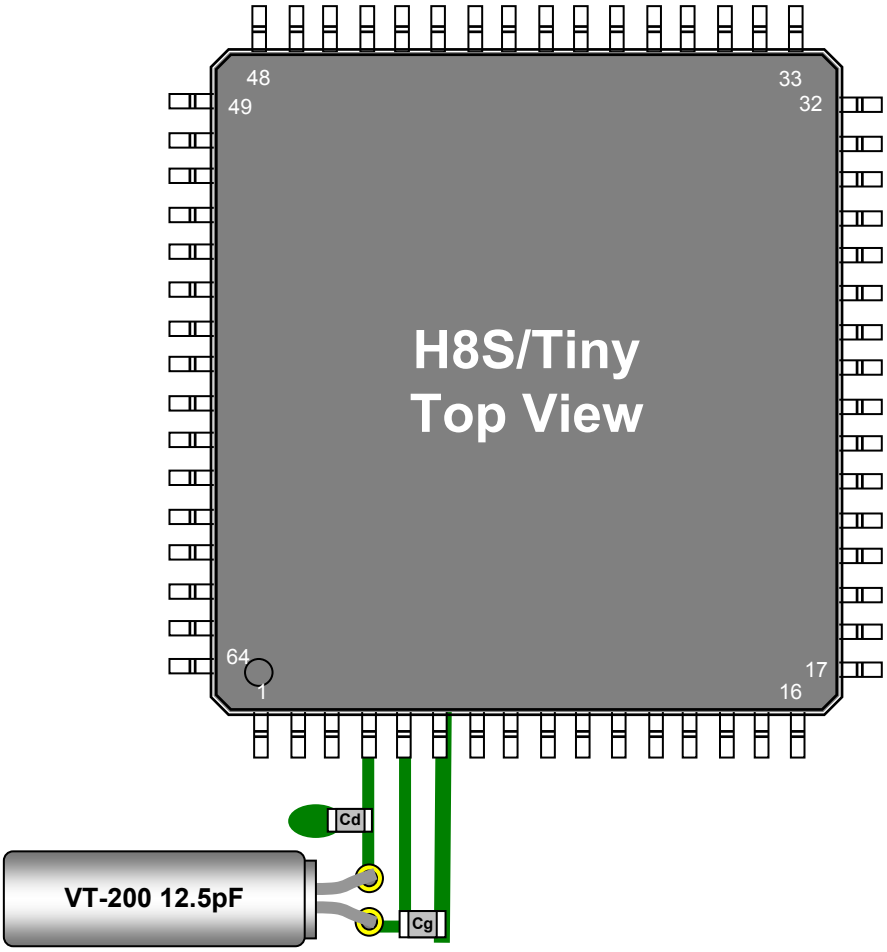

Figure 1 Referential components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.
Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

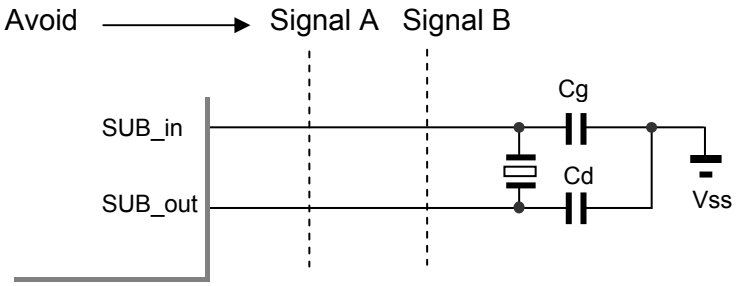

Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert a resistor, Rd, in series on the SUB_out side.

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Evaluation of Subsystem Clock Oscillation Circuit

VT-200 12.5pF with R4F20103NFB-64P [LQFP(14x14) 0.80mm pitch]

Measurement conditions : 5.0V

[Evaluation Sample at 25°C]

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
VT-200	1	12.5	32768.10	32765.24	29.2	0.89	2.338	71.2
	2	12.5	32768.18	32765.32	27.7	0.88	2.335	75.1
	3	12.5	32768.20	32765.33	28.0	0.88	2.344	74.1

[IC Test Data : IC Sample Rd=0 kohm,Cg=22pF,Cd=22pF at 25°C]

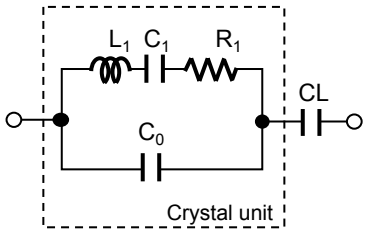
Lot.	IC Sample	Fosc(Hz)	df / f(x10^{-6})	DL(x10^{-6}W)	| -RL |(kohm)	Id (nA)	DC bias(V)	Vstart(V)	Ts(sec)
YBZ1200	TYP	32768.05	-1.53	0.09	1234	1,025	0.65	1.05	0.49
	HH	32767.97	-4.12	0.12	424	1,051	0.58	1.28	0.93
	LL	32768.10	0.09	0.08	1854	989	0.64	1.05	0.48
	LH	32768.04	-1.83	0.09	944	1,021	0.70	1.05	0.68
	HL	32768.03	-2.20	0.10	854	1,018	0.58	1.21	0.48

[IC Test Data : IC Sample Rd=0 kohm,Cg=22pF,Cd=22pF at 25°C]

Lot.	IC Sample	Fosc(Hz)	df / f(x10^{-6})	DL(x10^{-6}W)	| -RL |(kohm)	Id (nA)	DC bias(V)	Vstart(V)	Ts(sec)
YBZ1100	HH	32768.03	-2.14	0.09	1131	984	0.63	1.04	0.51
	LL	32768.05	-1.68	0.08	1331	987	0.62	1.04	0.57
	HL	32768.02	-2.44	0.09	1131	980	0.62	1.03	0.63
	LH	32768.03	-2.14	0.08	1331	980	0.63	1.05	0.53
	LS	32768.03	-2.29	0.09	1031	994	0.64	1.15	0.54
	LB	32768.05	-1.68	0.09	1131	1011	0.64	1.04	0.53

Remark (see figure 3)

$$Fo = fr \times \{ C1 / (2 \times (Co + CL)) + 1 \} \quad (Hz)$$



Fo : Load resonance frequency
fr : Resonance frequency
R1 : Motional resistance
C1 : Motional capacitance
Co : Shunt capacitance
CL : Load Capacitance

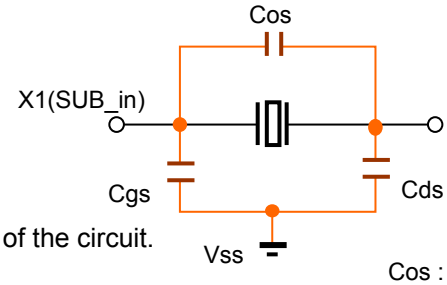
Figure 3 Equivalent circuit of crystal unit, and CL

Remark (see figure 4)

Approximate formula of the load capacitance of the circuit CL,

$$CL = Cg \times Cd / (Cg + Cd) + Cs \quad (pF)$$

where Cs(=2 to 4pF) stands for stray capacitance of the circuit.



Cos : X1_X2 Stray capacitance
Cgs : X1_Vss Stray capacitance
Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants differs depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

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Evaluation of Subsystem Clock Oscillation Circuit

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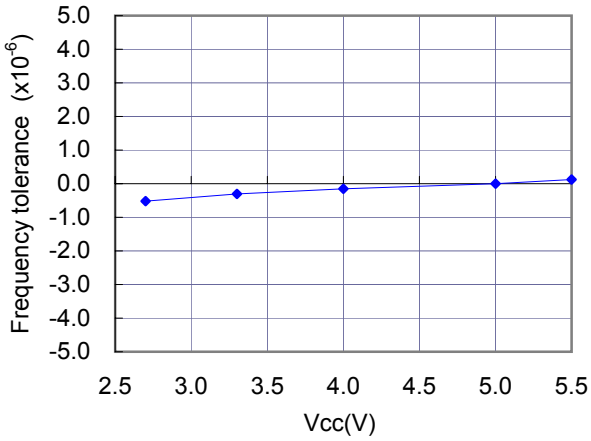
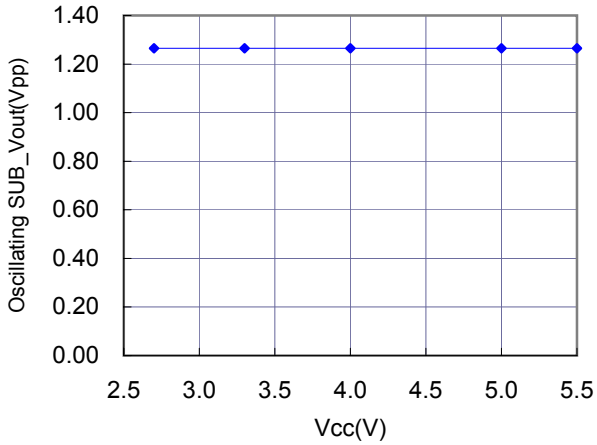
Measurement conditions : Vcc=2.7V to 5.5V at 25°C

Referential Data(1) : Voltage characteristics

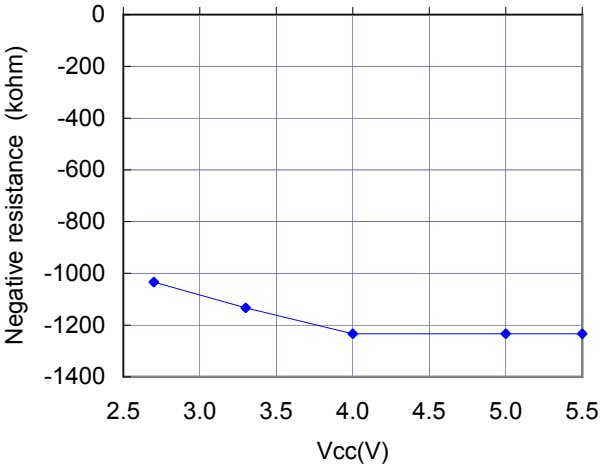
Frequency / voltage coefficient



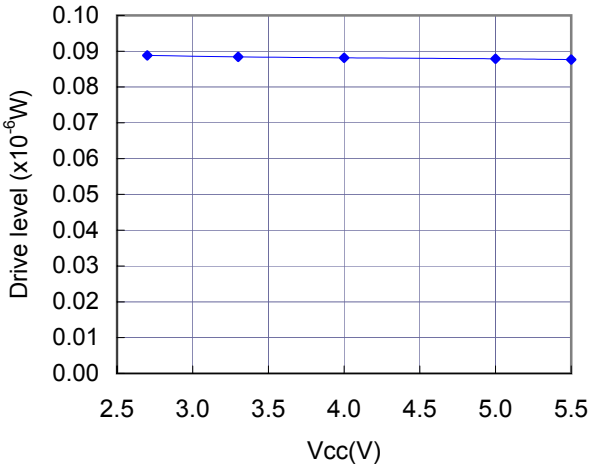
SUB_Vout / voltage coefficient



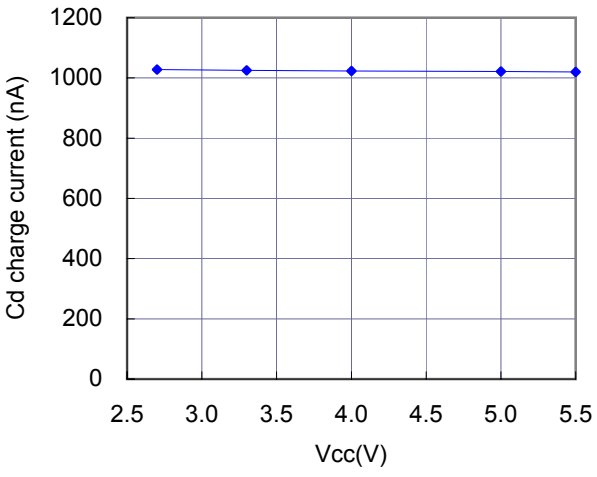
Negative resistance / voltage coefficient



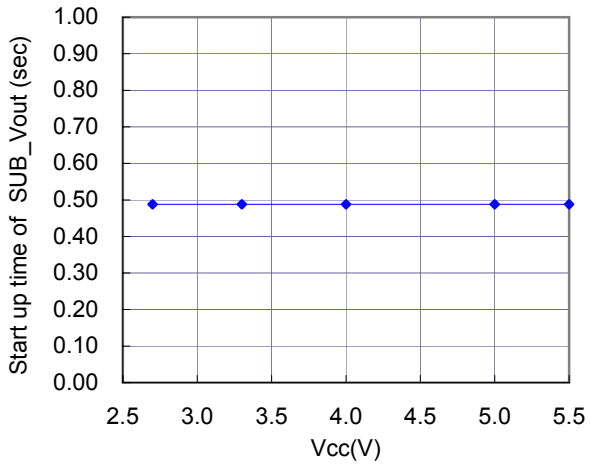
Drive level / voltage coefficient



Cd charge current / voltage coefficient



Start up time / voltage coefficient



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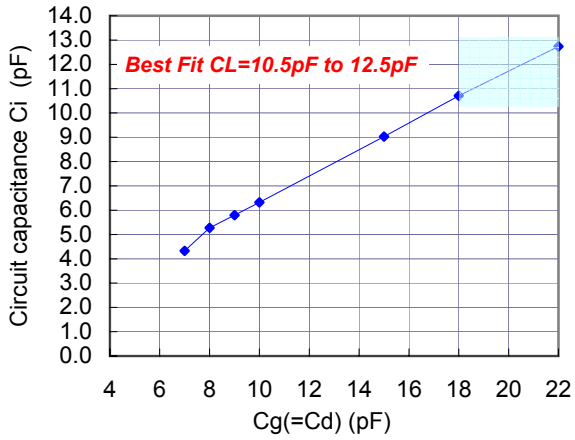
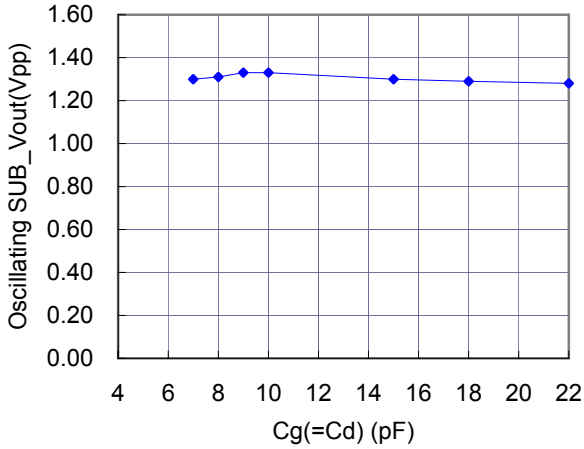
Measurement conditions : 5.0V at 25°C

Referential Data(2) : External capacitance Cg,Cd characteristics

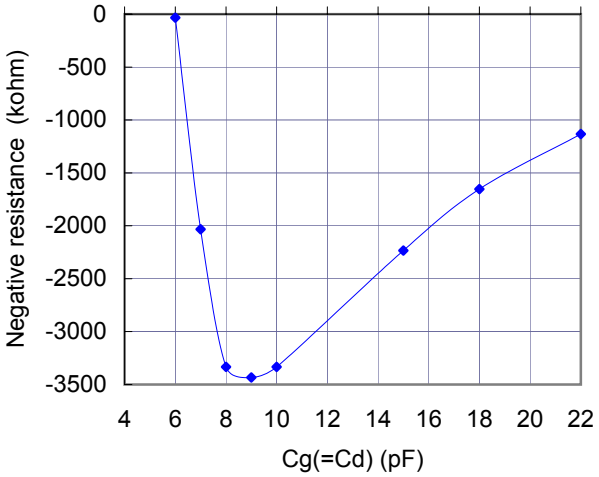
Circuit capacitance Ci / external Cg,Cd coefficient



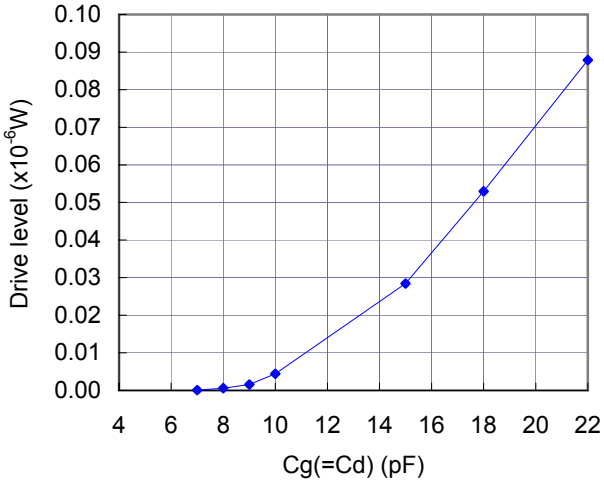
SUB_Vout / external Cg,Cd coefficient



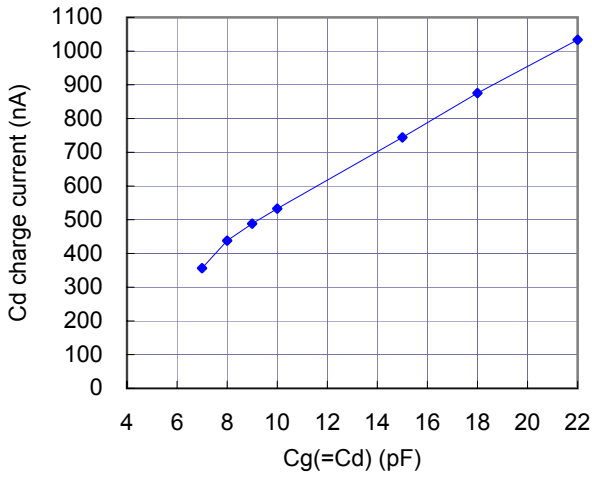
Negative resistance / external Cg,Cd coefficient



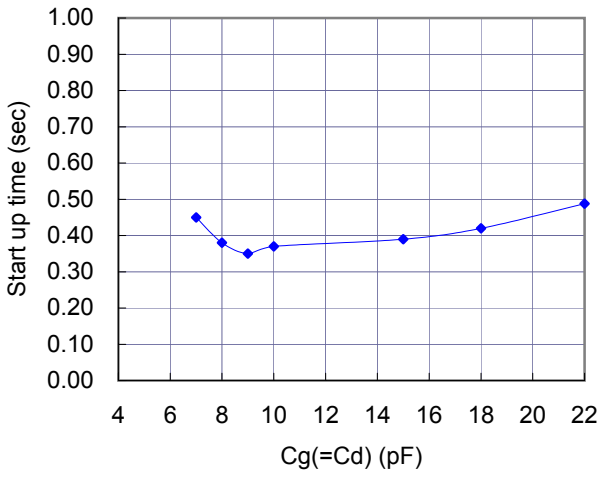
Drive level / external Cg,Cd coefficient



Cd charge current / external Cg,Cd coefficient



Start up time / external Cg,Cd coefficient



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