

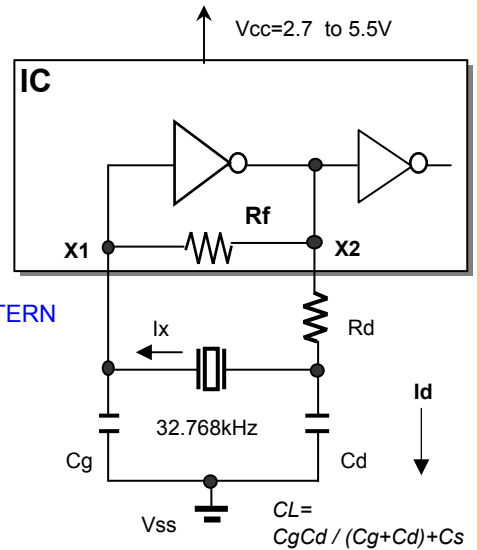
Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7 12.5pF with R4F20103NFB-64P [LQFP(14x14) 0.80mm pitch]

Measurement conditions : 3.3V ,5.0V



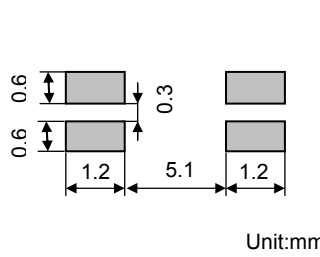
Model : SSP-T7
 Frequency : Fo=32.768kHz
 Frequency tolerance : dF/Fo= +/-20x10⁻⁶
 Load capacitance : CL=12.5pF
 Equivalent series resistance : R1=65kohm max
 Max. drive level : DL=1x10⁻⁶W max
 Level of drive : DL=0.1x10⁻⁶W typ



FEATURES

- 1.Ultra thin type with 1.4mm Max.
- 2.SMD type suitable for automatic & high density surface mounting.
- 3.Plastic mold package containing highly reliable tubular type quartz crystal.
- 4.Excellent shock and heat resistance.
- 5.Cellular phones,PDA,Radio communication equipment, Portable applications etc.

RECOMMENDED SOLDERING PATTERN



Remark) Ix : current through crystal

MODEL:SSP-T7 12.5pF with R4F20103NFB at 25°C

Key specifications	Vcc=3.3V	Vcc=5.0V	Remarks
Current control resistance : Rd (k ohm)	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	22	22	Optimal capacitance in response to CL
Capacitance at drain : Cd (pF)	22	22	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vcc=3.3V	Vcc=5.0V	Remarks
Matching Accuracy : df / f (x10 ⁻⁶)	-1.5	-1.2	Frequency offset volume at specified Vcc
Voltage Fluctuation : +/-df / V (x10 ⁻⁶)	0.1	0.1	Vcc +/-10% (Standard operating voltage range)
Drive Level : DL (x10 ⁻⁶ W)	0.10	0.10	DL=Ix ² Re < 1x10 ⁻⁶ W,Re=R1(1 + Co / CL) ²
Negative resistance : - RL (kohm)	1137	1237	5 times larger than R1MAX
Oscillation allowance : M (times)	17	19	Judgemental standard of oscillation stability
Normal consumption current : Id (nA)	1,019	1,019	Cd charge current, Id = ωCd*Vd
Voltage of oscillation start : Vstart (V)	1.05	1.05	
Voltage of oscillation stop : Vstop (V)	0.89	0.89	
Oscillation start up time : Ts (sec)	0.50	0.50	Time to reach 90% of output level

Temperature characteristics of circuit		Vcc=3.3V	Vcc=5.0V	Remarks
at -40°C	Variation : df / T (x10 ⁻⁶)	-140	-140	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)
at +85°C	Variation : df / T (x10 ⁻⁶)	-126	-126	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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We value the "takumi" spirit.

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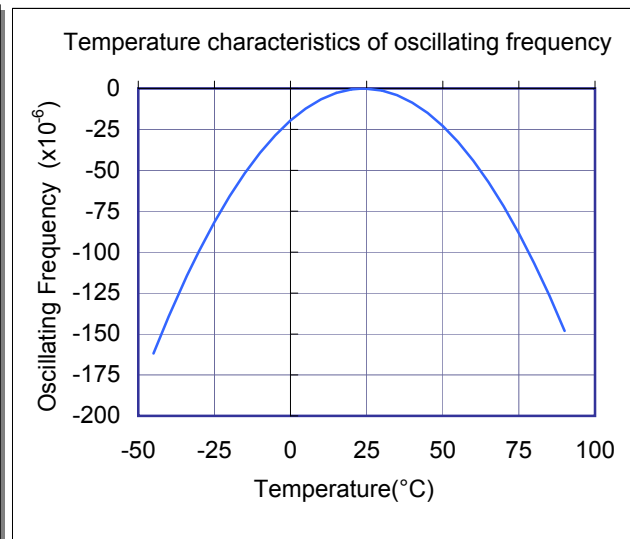
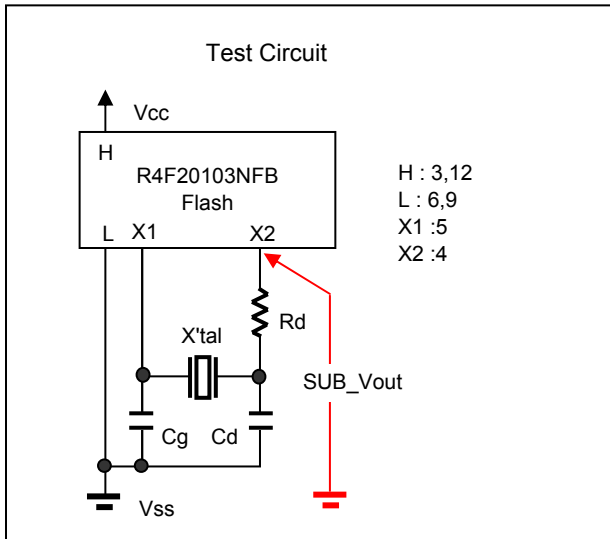
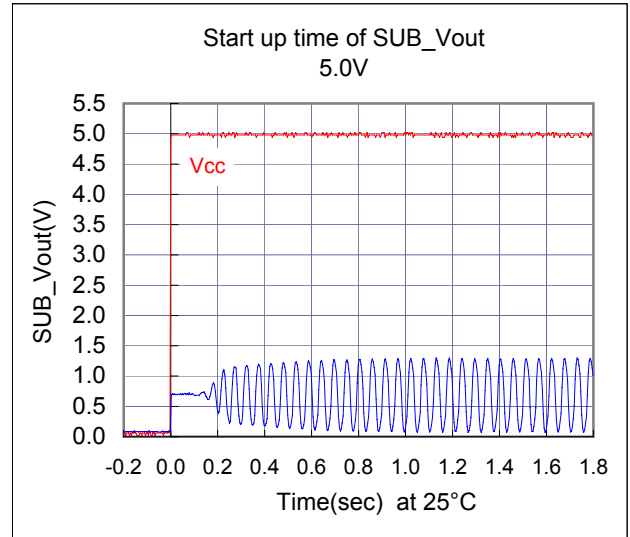
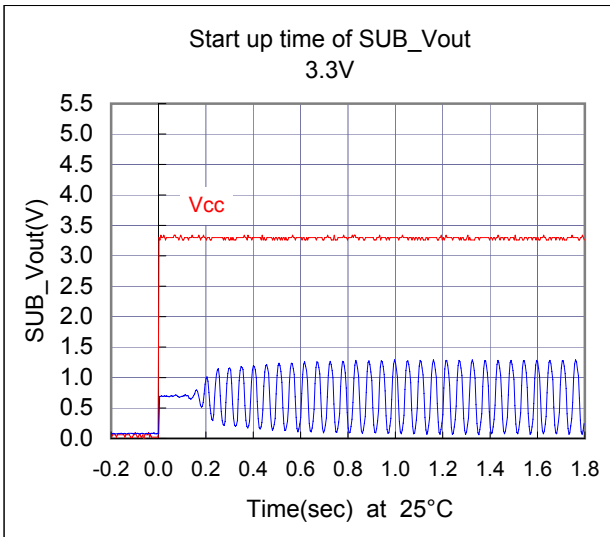
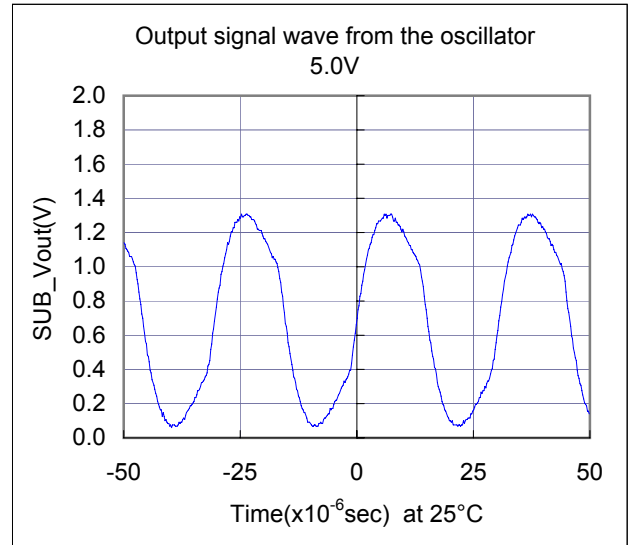
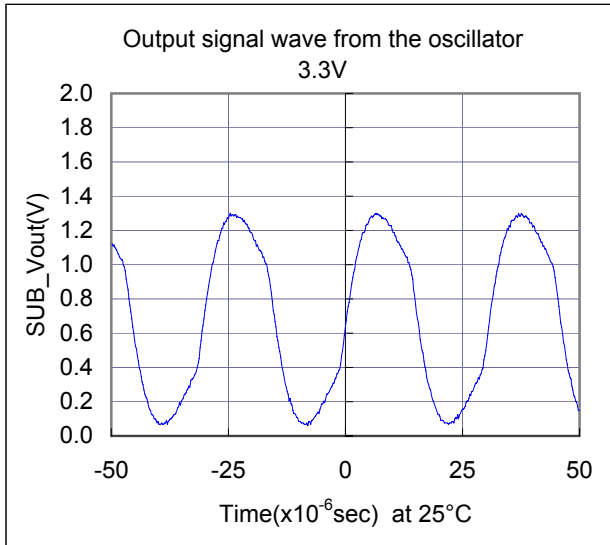
Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7 12.5pF with R4F20103NFB-64P [LQFP(14x14) 0.80mm pitch]

Measurement conditions : 3.3V ,5.0V



Test Data



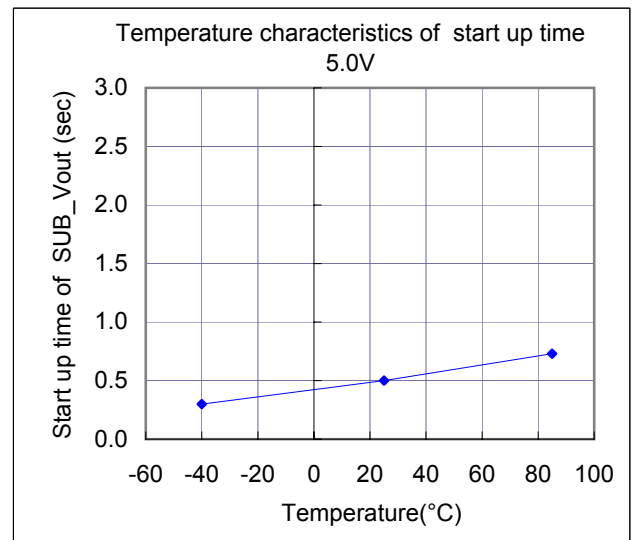
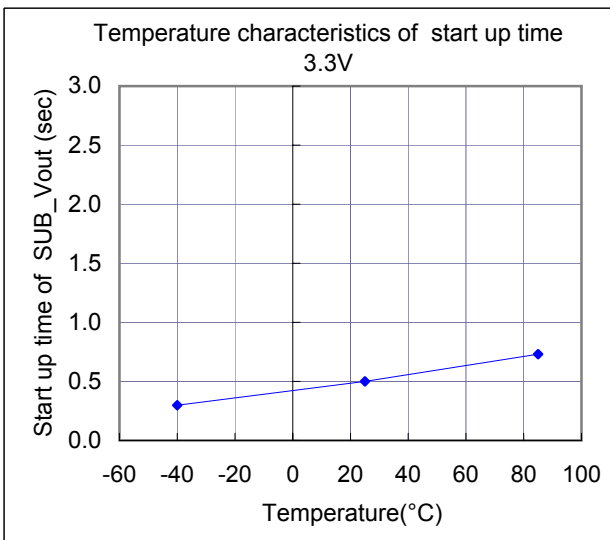
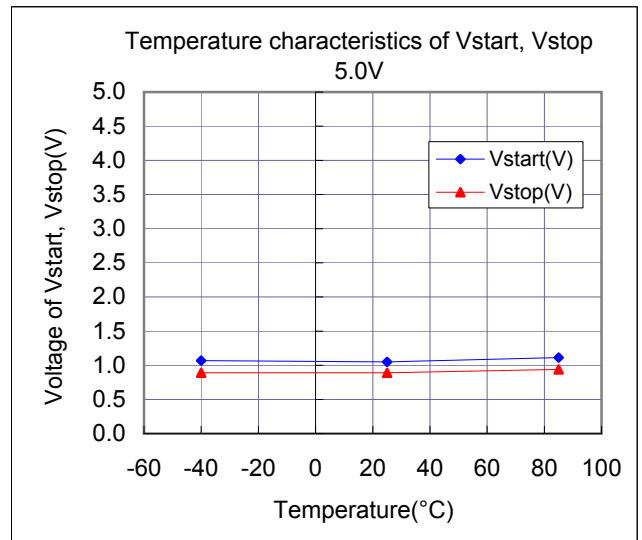
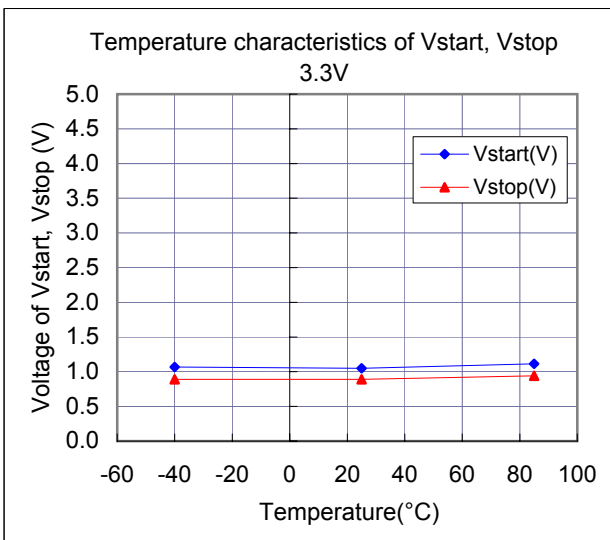
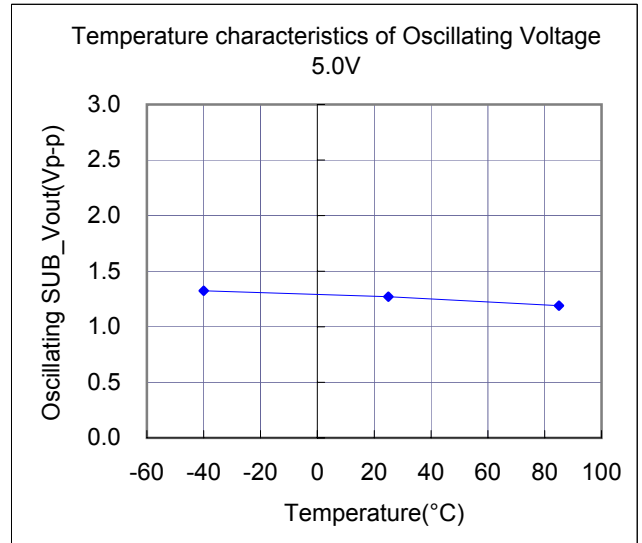
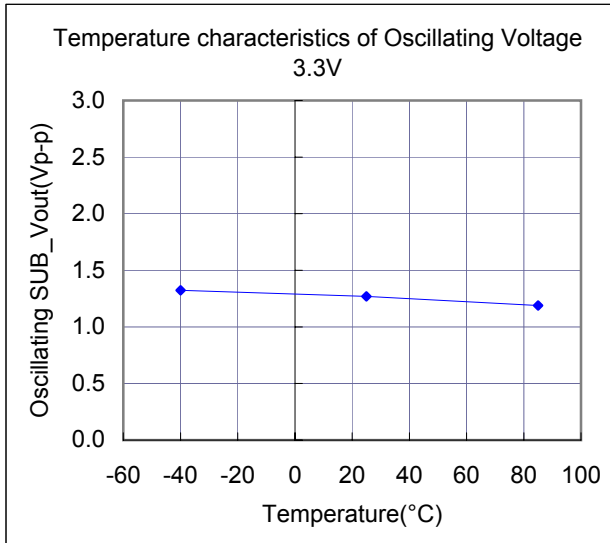
Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7 12.5pF with R4F20103NFB-64P [LQFP(14x14) 0.80mm pitch]

Measurement conditions : 3.3V ,5.0V



Test Data : Temperature characteristics



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SSP-T7 12.5pF with R4F20103NFB-64P [LQFP(14x14) 0.80mm pitch]

Measurement conditions : 3.3V ,5.0V



Referential components layout(see Figure 1)

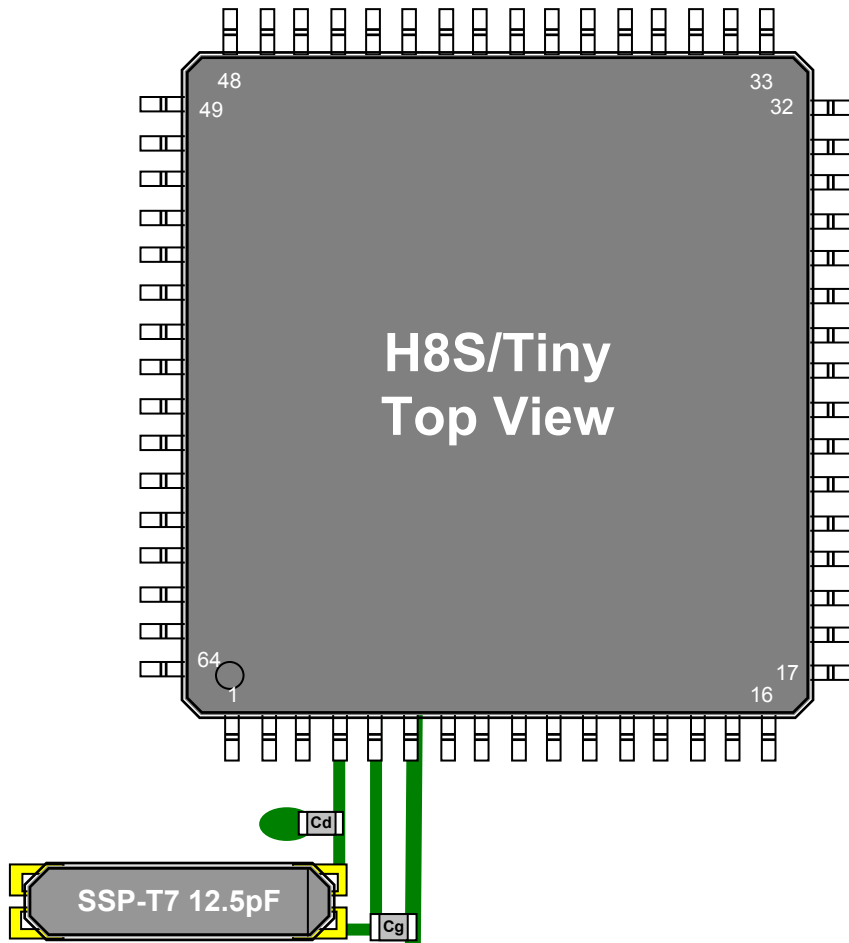


Figure 1 Referential components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

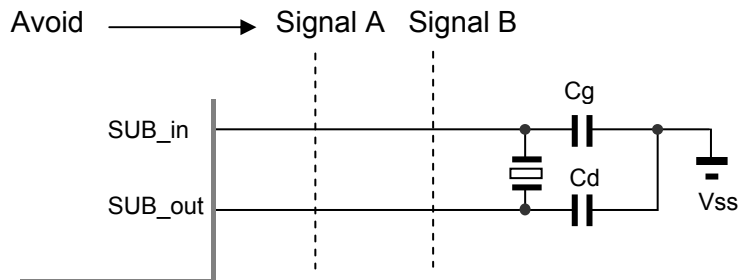


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert a resistor, Rd, in series on the SUB_out side.

Evaluation of Subsystem Clock Oscillation Circuit

SSP-T7 12.5pF with R4F20103NFB-64P [LQFP(14x14) 0.80mm pitch]

Measurement conditions : 5.0V



[Evaluation Sample at 25°C]

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
SSP-T7	1	12.5	32768.09	32765.44	32.0	0.89	2.166	70.1
	2	12.5	32768.18	32765.52	35.0	0.90	2.176	63.8
	3	12.5	32767.84	32765.20	34.3	0.90	2.159	65.6

[IC Test Data : IC Sample Rd=0 kohm,Cg=22pF,Cd=22pF at 25°C]

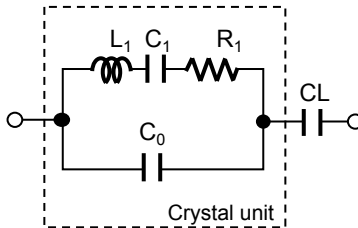
Lot.	IC Sample	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Id (nA)	DC bias(V)	Vstart(V)	Ts(sec)
YBZ1200	TYP	32768.05	-1.22	0.10	1237	1,023	0.65	1.05	0.50
	HH	32767.97	-3.81	0.13	427	1,051	0.58	1.28	0.93
	LL	32768.10	0.40	0.09	1857	985	0.64	1.05	0.48
	LH	32768.04	-1.53	0.10	947	1,019	0.70	1.05	0.68
	HL	32768.03	-1.89	0.11	857	1,016	0.58	1.21	0.48

[IC Test Data : IC Sample Rd=0 kohm,Cg=22pF,Cd=22pF at 25°C]

Lot.	IC Sample	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Id (nA)	DC bias(V)	Vstart(V)	Ts(sec)
YBZ1100	HH	32768.03	-1.83	0.10	1137	982	0.63	1.04	0.51
	LL	32768.05	-1.37	0.10	1337	984	0.62	1.04	0.57
	HL	32768.02	-2.14	0.10	1137	978	0.62	1.03	0.63
	LH	32768.03	-1.83	0.10	1337	978	0.63	1.05	0.53
	LS	32768.03	-1.98	0.10	1037	993	0.64	1.15	0.54
	LB	32768.05	-1.37	0.10	1137	1009	0.64	1.04	0.53

Remark (see figure 3)

$$F_o = f_r \times \{ C_1 / (2 \times (C_o + C_L)) + 1 \} \text{ (Hz)}$$



- Fo : Load resonance frequency
- fr : Resonance frequency
- R1 : Motional resistance
- C1 : Motional capacitance
- Co : Shunt capacitance
- CL : Load Capacitance

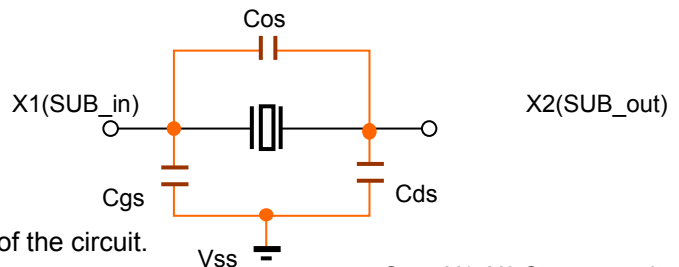
Figure 3 Equivalent circuit of crystal unit, and CL

Remark (see figure 4)

Approximate formula of the load capacitance of the circuit CL,

$$C_L = C_g \times C_d / (C_g + C_d) + C_s \text{ (pF)}$$

where Cs(=2 to 4pF) stands for stray capacitance of the circuit.



- Cos : X1_X2 Stray capacitance
- Cgs : X1_Vss Stray capacitance
- Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants differs depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

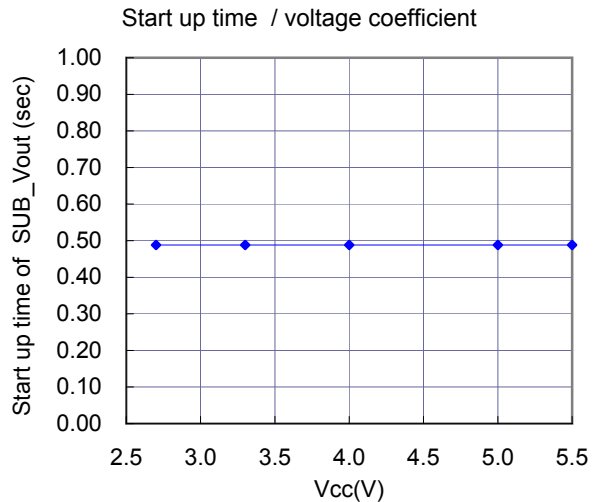
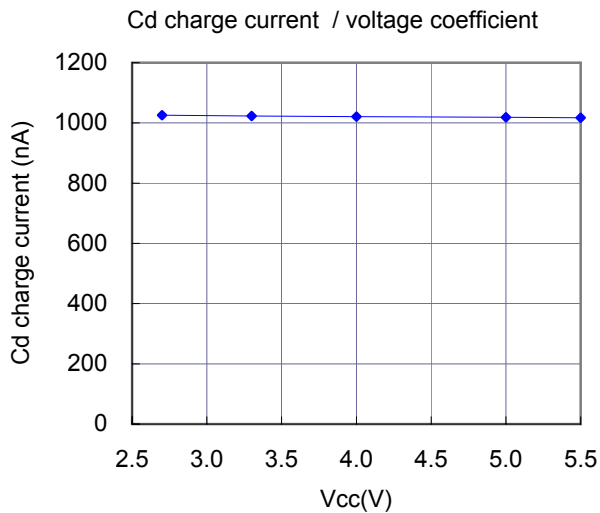
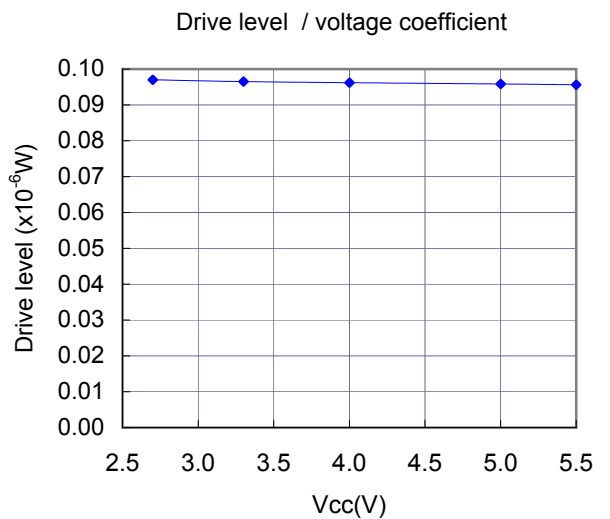
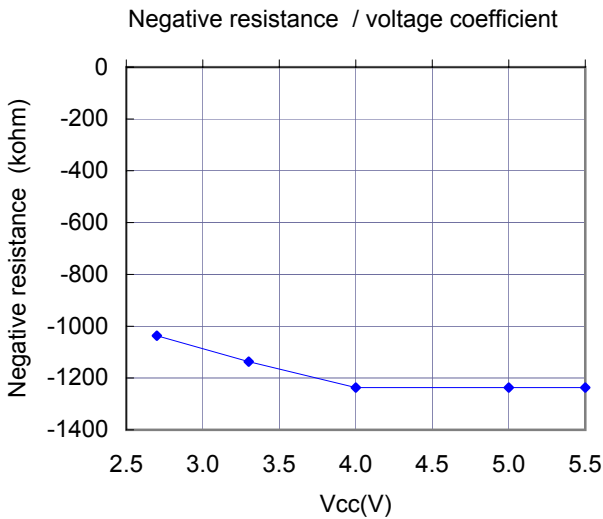
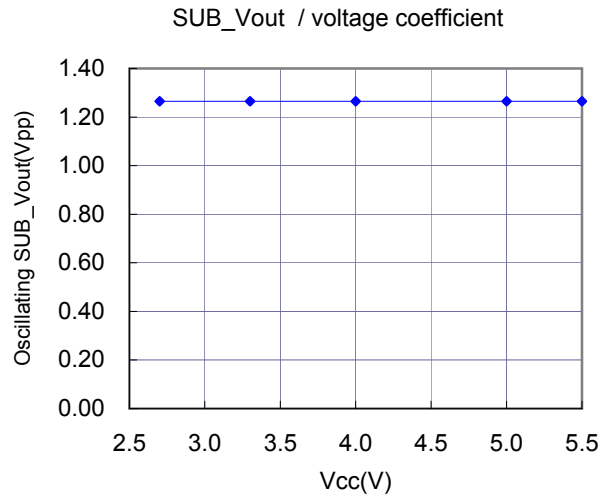
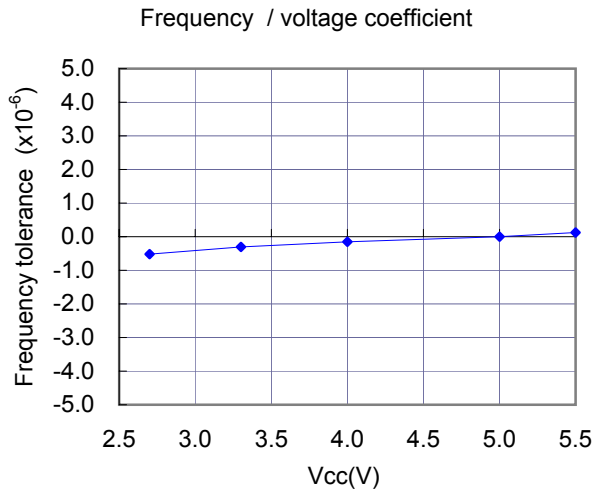
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SSP-T7 12.5pF with R4F20103NFB-64P [LQFP(14x14) 0.80mm pitch]

Measurement conditions : Vcc=2.7V to 5.5V at 25°C



Referential Data(1) : Voltage characteristics



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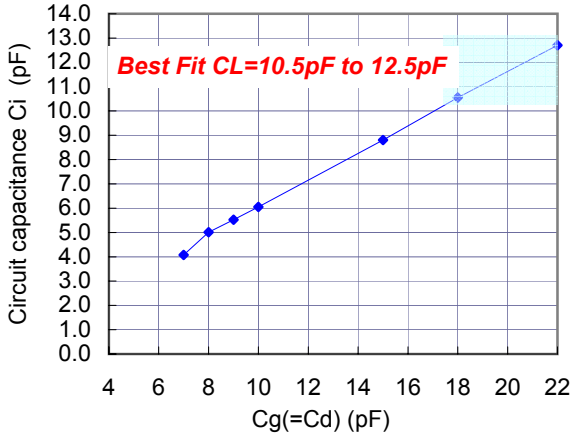
SSP-T7 12.5pF with R4F20103NFB-64P [LQFP(14x14) 0.80mm pitch]

Measurement conditions : 5.0V at 25°C

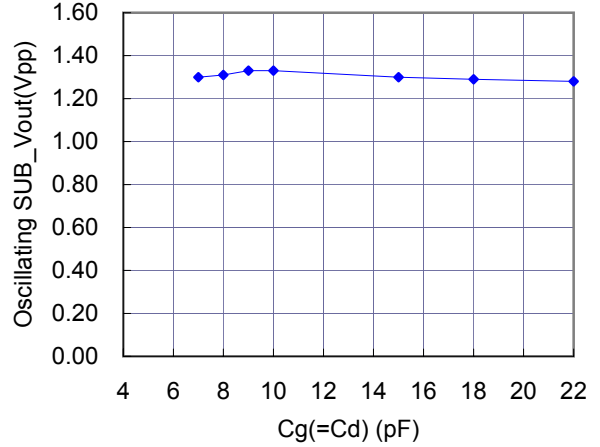


Referential Data(2) : External capacitance Cg,Cd characteristics

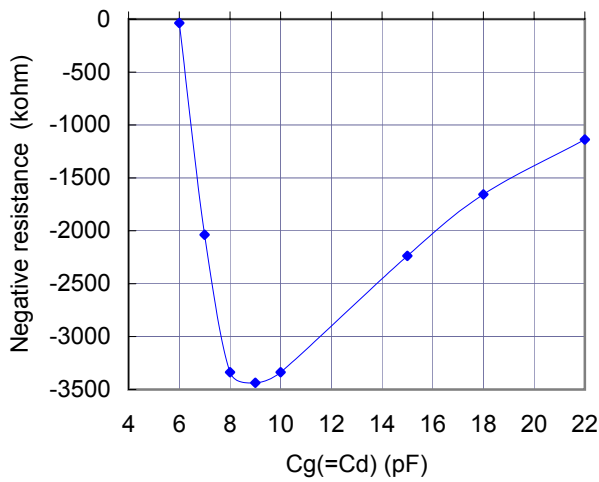
Circuit capacitance Ci / external Cg,Cd coefficient



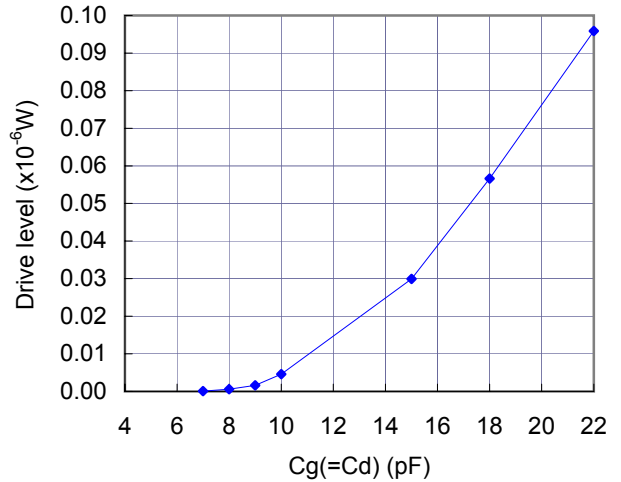
SUB_Vout / external Cg,Cd coefficient



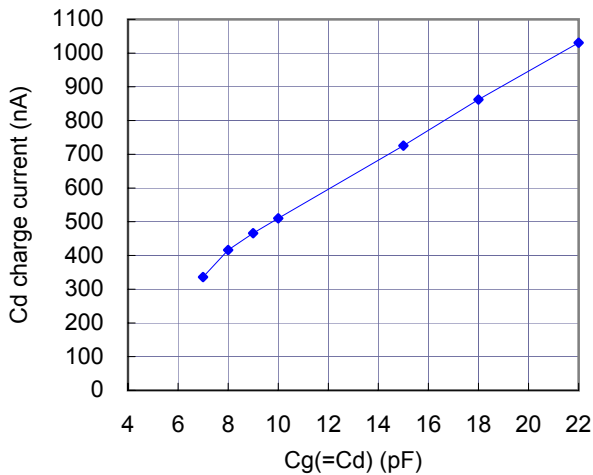
Negative resistance / external Cg,Cd coefficient



Drive level / external Cg,Cd coefficient



Cd charge current / external Cg,Cd coefficient



Start up time / external Cg,Cd coefficient

