

Evaluation of a Low Frequency Clock Oscillation Circuit

VT-200-FL 3.7pF with uPD78F1009GB-16BT [LQFP(10x10) 0.50mm pitch]

Measurement conditions : 3.0V



New

VT-200-FL

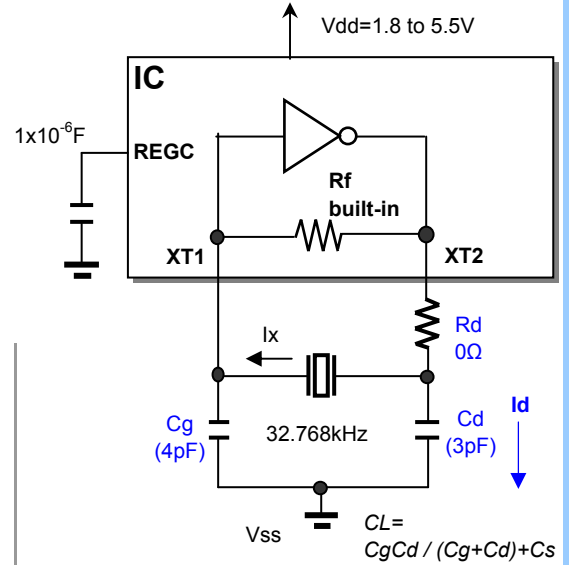
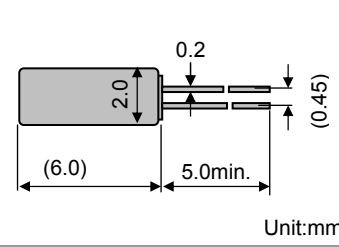


Model :VT-200-FL
 Frequency :Fo=32.768kHz
 Frequency tolerance :dF/Fo= +/-20x10⁻⁶
 Load capacitance :CL=3.7pF
 Equivalent series resistance :R1=50kΩ max
 Max. drive level :DL=1μW max
 Level of drive :DL=0.01μW typ

FEATURES

- 1.Compact tubular package
- 2.Photolithographic process
- 3.Excellent shock resistance and environmental characteristics.
- 4.Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)



Remark) Ix : current through crystal

Extremely low power consumption 78K0R/Kx3-L and VT-200-FL 3.7pF

*1 ; Low current consumption mode (default)

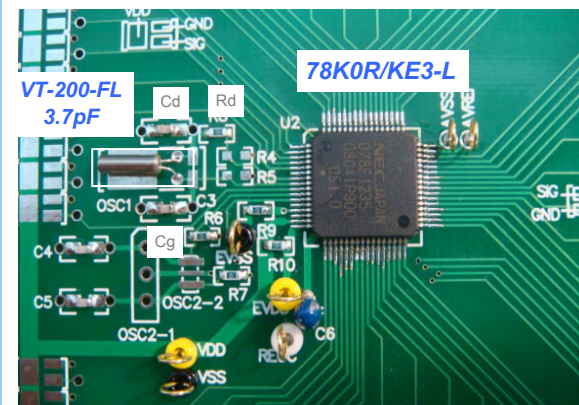
*2 ; Extremely low current consumption mode

MODEL:VT-200-FL 3.7pF with uPD78F1009GB at 25°C

Key specifications	Low(*2)	Low(*1)	Remarks
Current control resistance : Rd (kΩ)	0	0	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	4	4	Optimal capacitance in response to CL
Capacitance at drain : Cd (pF)	3	3	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Low(*2)	Low(*1)	Remarks
Matching Accuracy : df / f (x10 ⁻⁶)	0.7	1.5	Frequency offset volume at specified Vdd
Voltage Fluctuation : +/-df / V (x10 ⁻⁶)	0.0	0.0	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL (μ W)	0.005	0.004	DL=Ix ² Re < 1x10 ⁻⁶ W, Re=R1(1 + Co / CL) ²
Negative resistance : - RL (kΩ)	970	1360	5 times larger than R _{1MAX}
Oscillation allowance : M (times)	19	27	Judgmental standard of oscillation stability
Low current consumption : Id (nA)	89	156	Cd charge current, Id = ωCd*Vd < 200nA
Voltage of oscillation start : Vstart (V)	1.63	1.63	
Voltage of oscillation stop : Vstop (V)	1.59	1.59	
Oscillation start up time : Ts (sec)	0.64	0.47	Time to reach 90% of output level<1.5sec

Temperature characteristics of circuit		Low(*2)	Low(*1)	Remarks
at -40°C	Variation : df / T (x10 ⁻⁶)	-143	-143	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)
at +85°C	Variation : df / T (x10 ⁻⁶)	-121	-121	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)



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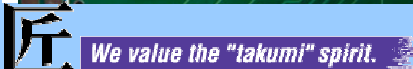
2990,West Lomita Blvd., Torrance, CA 90505, U.S.A
 Telephone :+1 310-517-7771 Facsimile :+1 310-517-7792
 Email :info@siu-la.com

Seiko Instruments GmbH

Siemensstrasse 9,D-63263 Neu-Isenburg,Germany
 Telephone :+49-6102-297-0 Facsimile :+49-6102-297-320
 Email :info@seiko-instruments.de

Seiko Instruments Inc.

1-8,Nakase,Mihama-ku,Chiba-shi,Chiba 261-8507,Japan
 Facsimile :+81-43-211-8030
 E-mail :component@sii.co.jp



Seiko Instruments Inc.
 Phone:+81-43-211-1207(Direct)

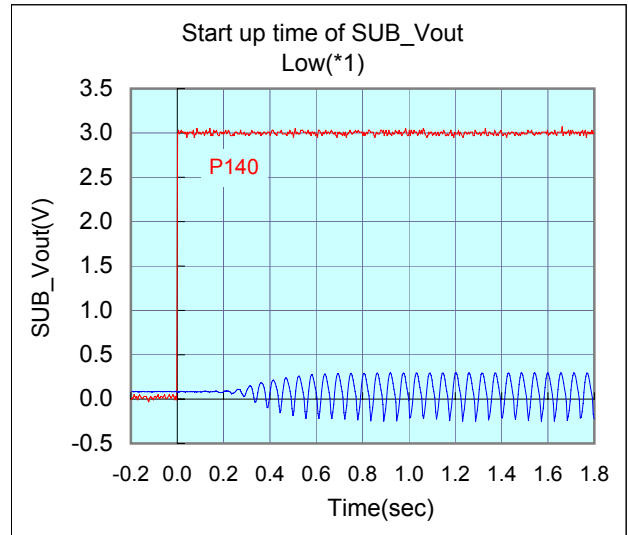
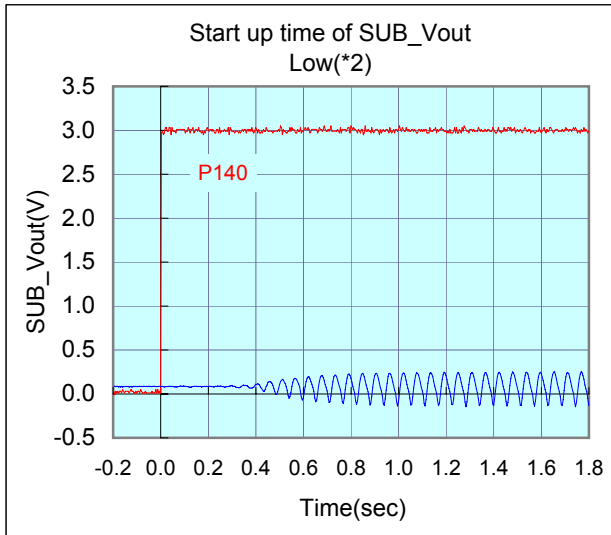
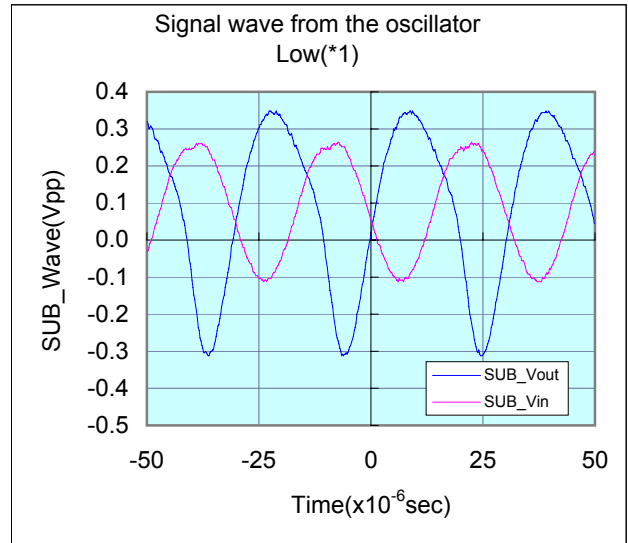
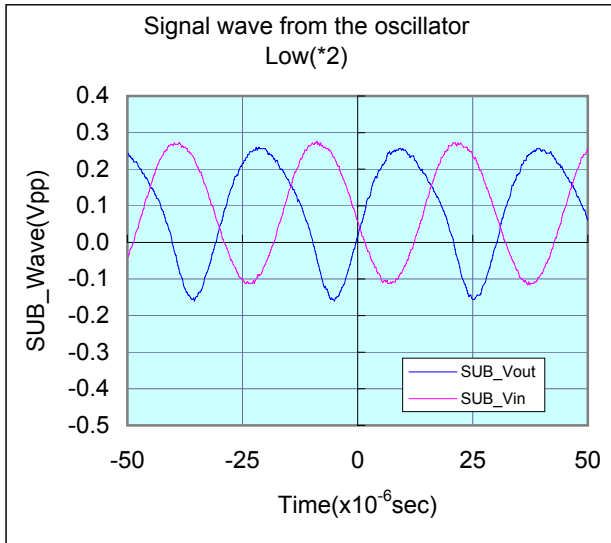
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Measurement conditions : 3.0V

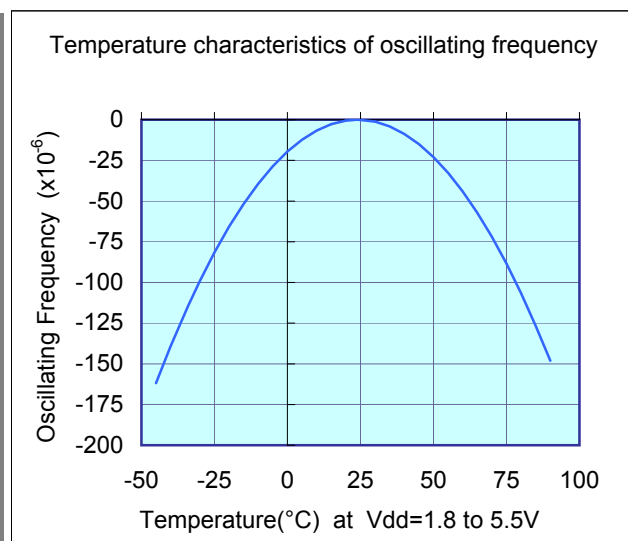
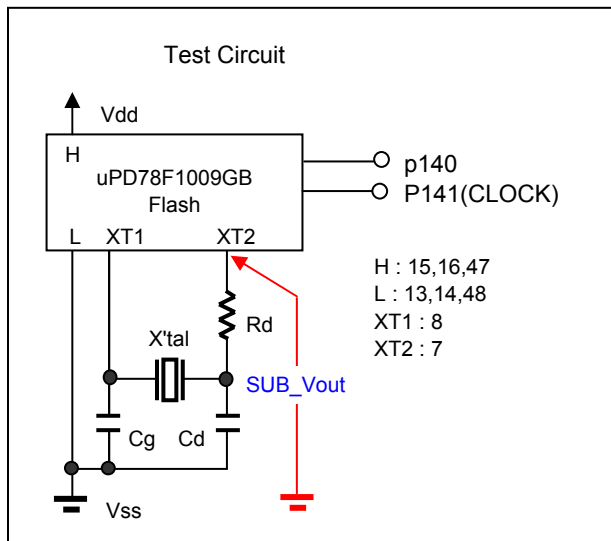


Test Data at 25°C



*2 ; Extremely low current consumption mode

*1 ; Low current consumption mode



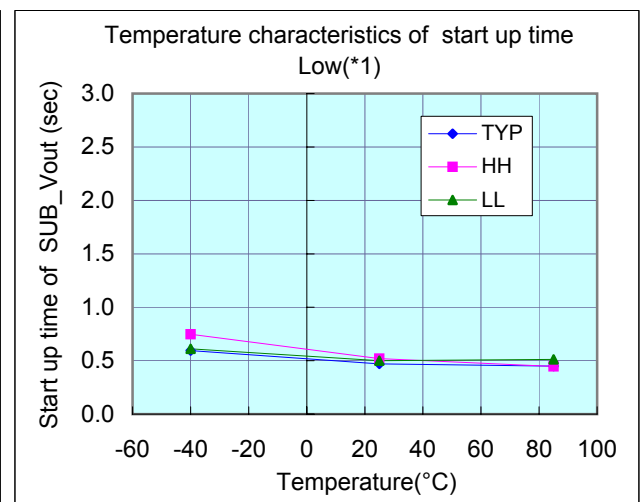
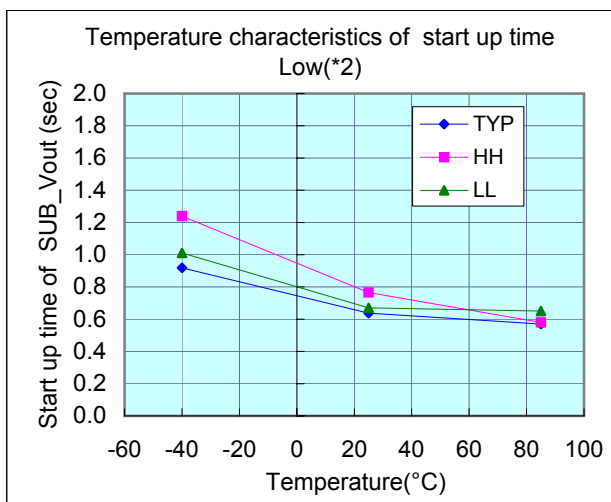
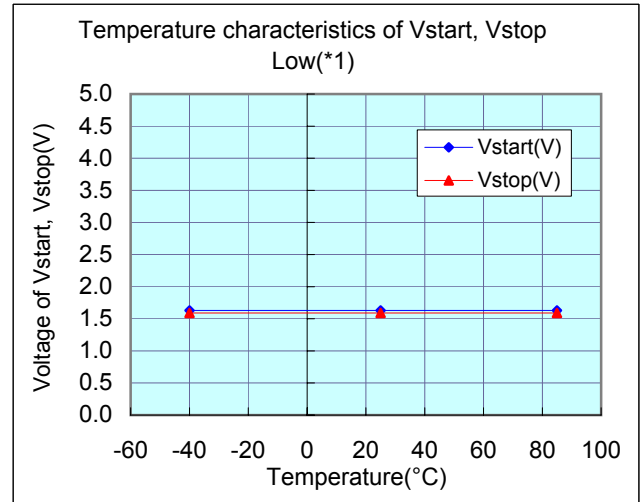
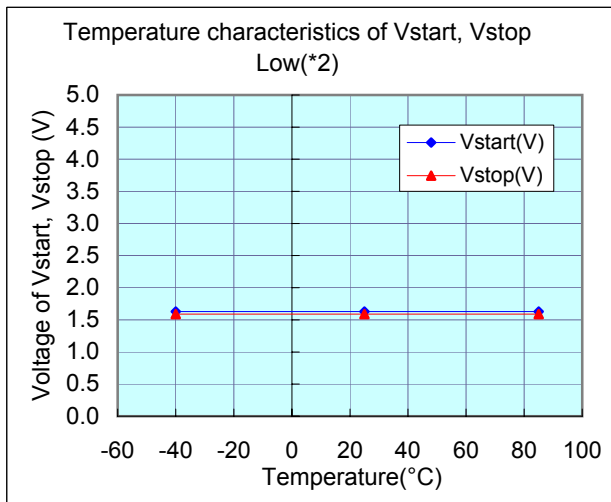
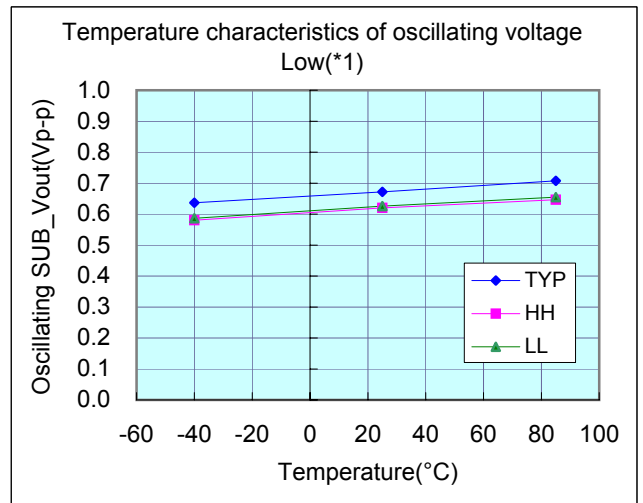
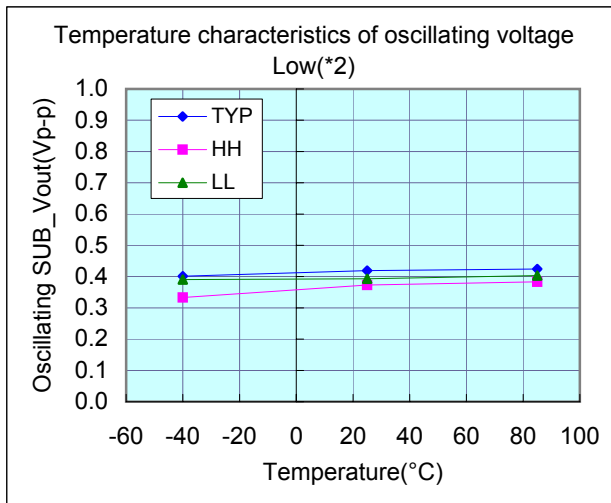
Evaluation of a Low Frequency Clock Oscillation Circuit

VT-200-FL 3.7pF with uPD78F1009GB-16BT [LQFP(10x10) 0.50mm pitch]

Measurement conditions : 3.0V



Test Data : Temperature characteristics



*2 ; Extremely low current consumption mode

*1 ; Low current consumption mode

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

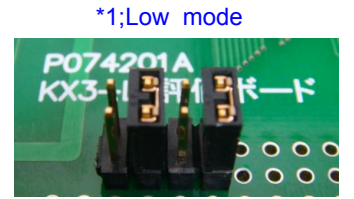
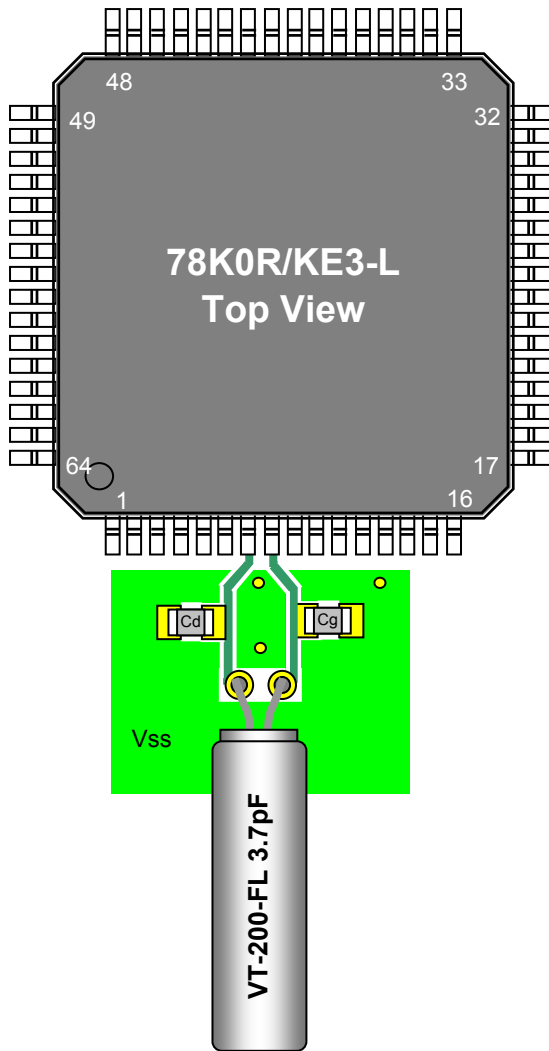
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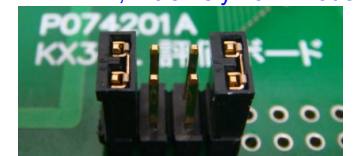
Measurement conditions : 3.0V



Referential components layout(see Figure 1)



*1;Low mode



*2;Extremely Low mode

- Vdd:15 (H)
- EVdd:16(H)
- AVREF:47(H)
- AVss:48 (L)
- Vss:13(L)
- Evss:14(L)
- FLMD0:9(L)
- XT1:8 (SUB_in)
- XT2:7 (SUB_out)
- RESET:6
- REGC:12
- P140:64

Figure 1 Referential components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

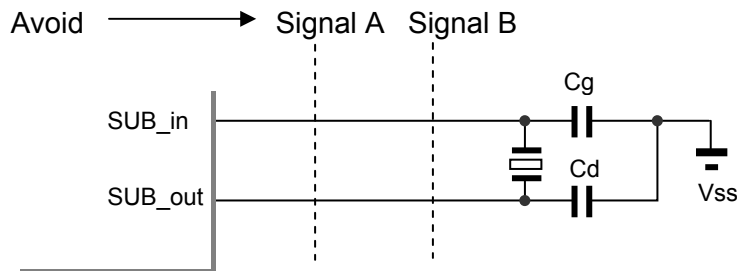


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert a resistor, Rd, in series on the SUB_out side.

Evaluation of a Low Frequency Clock Oscillation Circuit

VT-200-FL 3.7pF with uPD78F1009GB-16BT [LQFP(10x10) 0.50mm pitch]

Measurement conditions : 3.0V

**[Evaluation Sample at 25°C]**

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kΩ)	Co(pF)	C1(fF)	Q(k)
VT-200-FL	1	3.7	32767.95	32760.44	43.8	0.89	2.107	52.7
	2	3.7	32767.99	32760.52	38.7	0.90	2.099	59.8
	3	3.7	32767.97	32760.47	42.0	0.90	2.105	55.0

[IC Test Data : IC Sample Rd=0 Ω,Cg=4pF,Cd=3pF at 25°C]

Power mode	IC Sample	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(μW)	-RL (kΩ)	M(times)	Id (nA)	Vstart(V)	Ts(sec)
Low(*1)	TYP	32768.05	1.53	0.004	1360	27	156	1.63	0.47
	HH	32768.05	1.65	0.006	1360	27	144	1.63	0.52
	LL	32768.02	0.67	0.004	1260	25	146	1.63	0.50
	HL	32768.05	1.56	0.006	1160	23	148	1.63	0.53
	LH	32768.05	1.53	0.004	1360	27	149	1.63	0.49

*1; Low current consumption mode

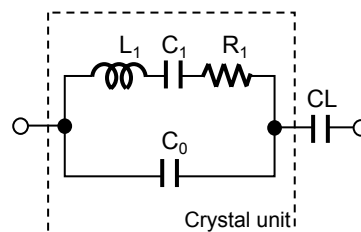
[IC Test Data : IC Sample Rd=0 Ω,Cg=4pF,Cd=3pF at 25°C]

Power mode	IC Sample	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(μW)	-RL (kΩ)	M(times)	Id (nA)	Vstart(V)	Ts(sec)
Low(*2)	TYP	32768.02	0.67	0.005	970	19	89	1.63	0.64
	HH	32768.00	0.00	0.005	970	19	80	1.63	0.77
	LL	32768.01	0.37	0.004	970	19	84	1.63	0.67
	HL	32768.01	0.40	0.005	880	18	83	1.63	0.80
	LH	32768.02	0.61	0.004	970	19	86	1.63	0.65

*2; Extremely low current consumption mode

Remark (see figure 3)

$$F_o = f_r \times \left\{ \frac{C_1}{2 \times (C_o + C_L)} + 1 \right\} \quad (\text{Hz})$$



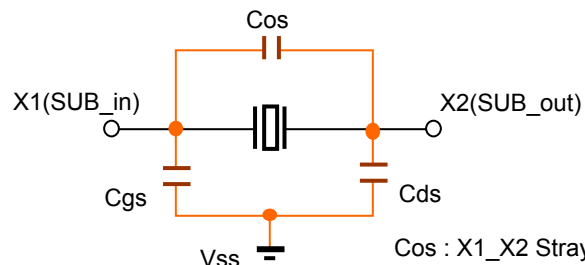
F_o : Load resonance frequency
 f_r : Resonance frequency
 R_1 : Motional resistance
 C_1 : Motional capacitance
 C_o : Shunt capacitance
 C_L : Load Capacitance

Figure 3 Equivalent circuit of crystal unit, and CL**Remark (see figure 4)**

Approximate formula of the load capacitance of the circuit CL,

$$C_L = C_g \times C_d / (C_g + C_d) + C_s \quad (\text{pF})$$

$$C_s = C_{gs} \times C_{ds} / (C_{gs} + C_{ds}) + C_{os} \quad (\text{pF})$$



C_{os} : X1_X2 Stray capacitance
 C_{gs} : X1_Vss Stray capacitance
 C_{ds} : X2_Vss Stray capacitance

where C_s (=1.5 to 2.5pF) stands for stray capacitance of the circuit.

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.



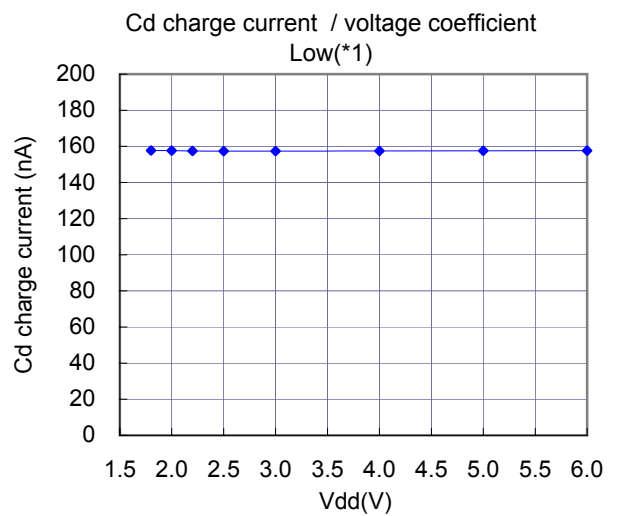
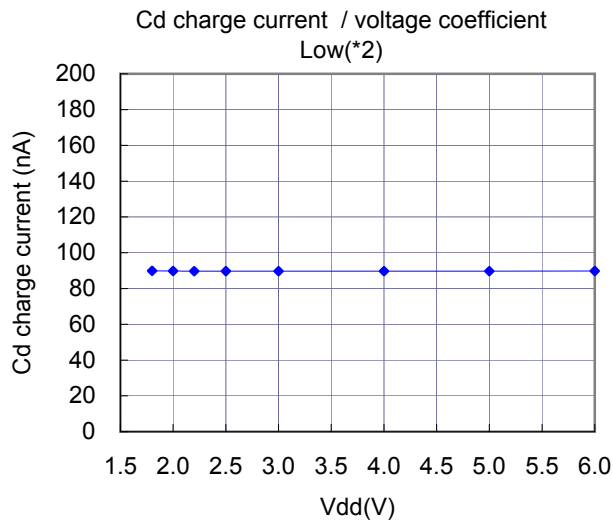
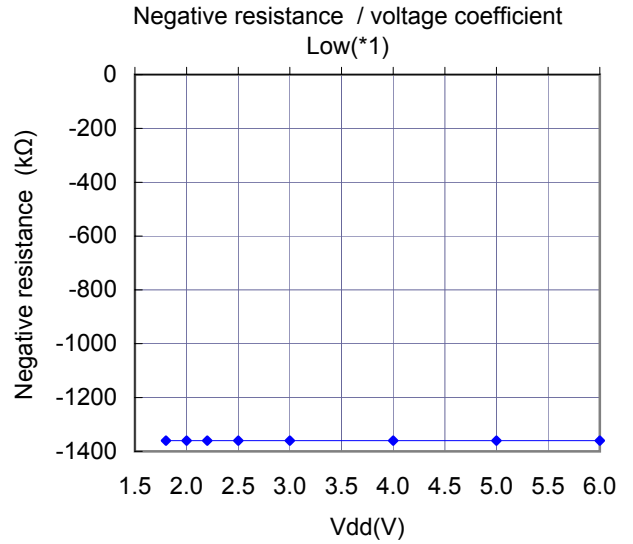
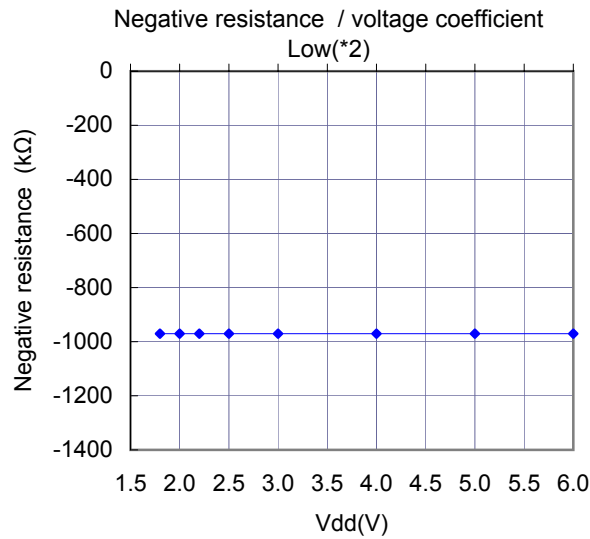
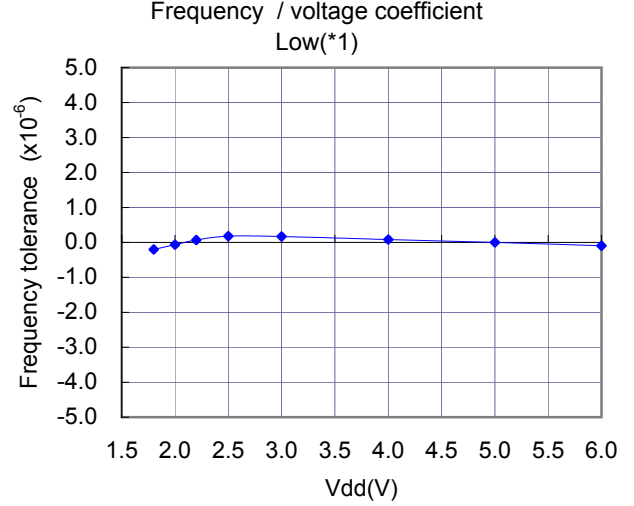
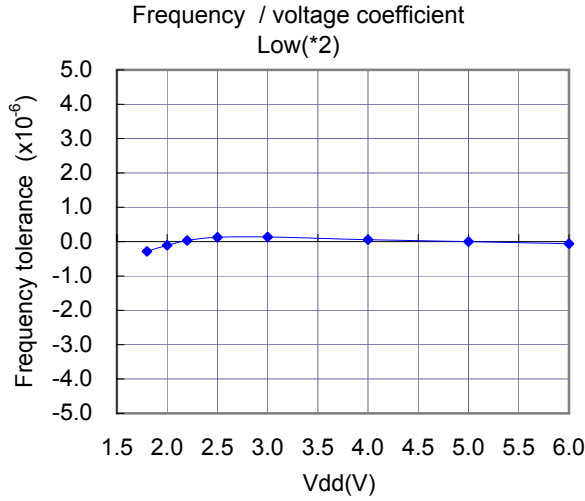
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VT-200-FL 3.7pF with uPD78F1009GB-16BT [LQFP(10x10) 0.50mm pitch]

Measurement conditions : Vdd=1.8V to (6.0)V at 25°C



Referential Data(1): Voltage characteristics



*2 ; Extremely low current consumption mode

*1 ; Low current consumption mode

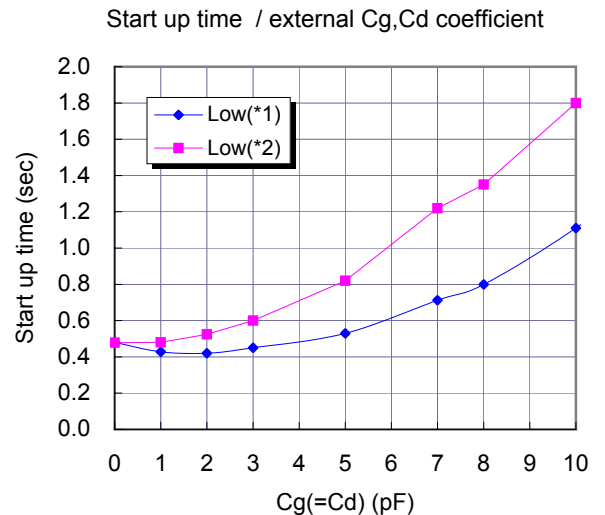
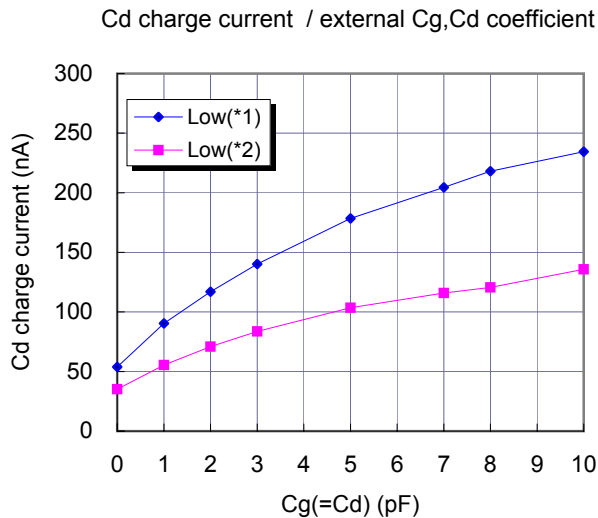
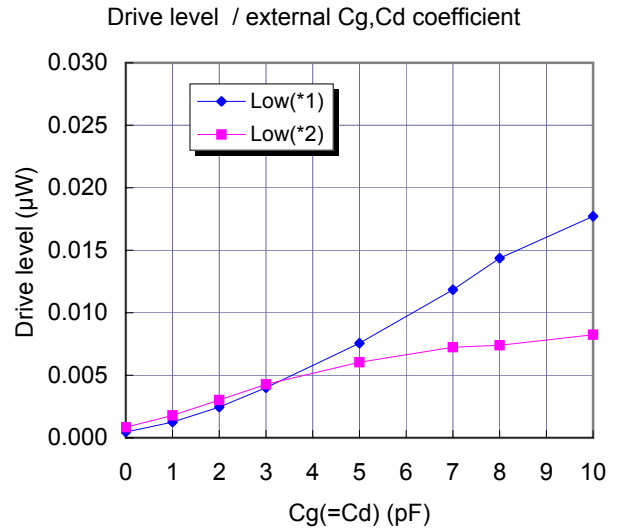
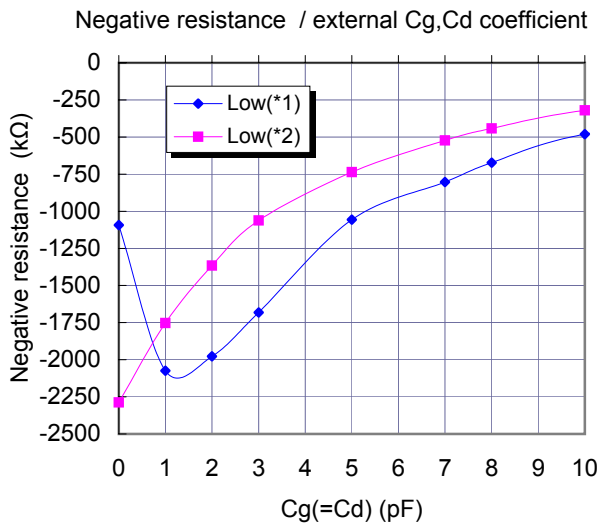
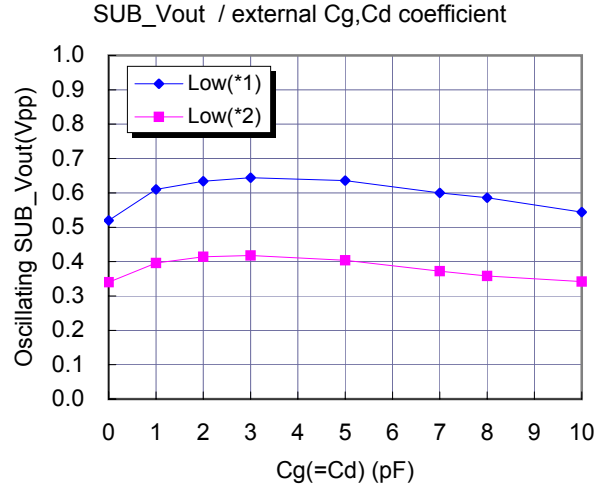
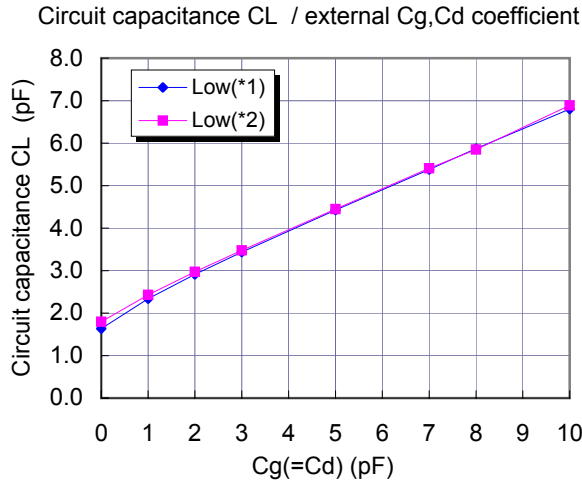
Evaluation of a Low Frequency Clock Oscillation Circuit

VT-200-FL 3.7pF with uPD78F1009GB-16BT [LQFP(10x10) 0.50mm pitch]

Measurement conditions : Vdd=1.8V to 5.5V at 25°C



Referential Data(2) : External capacitance Cg,Cd characteristics



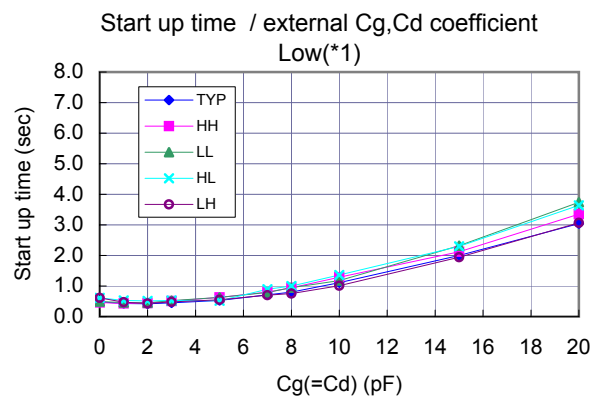
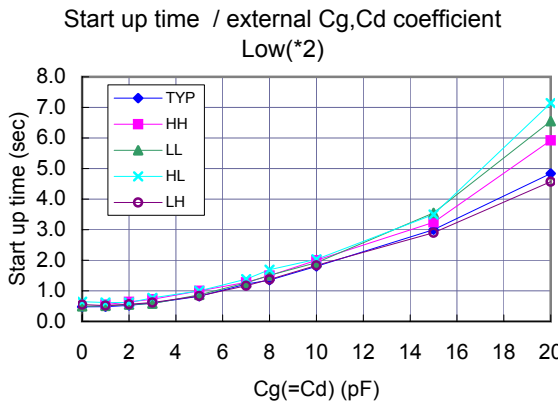
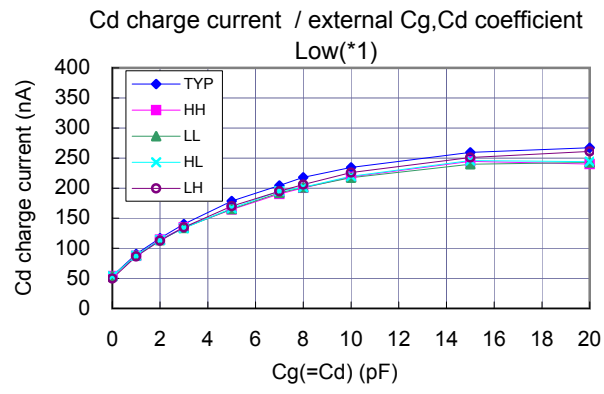
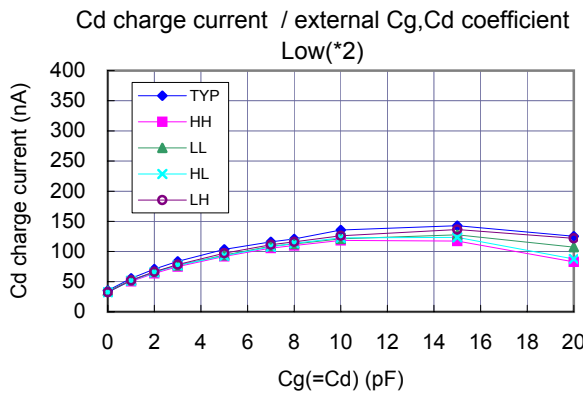
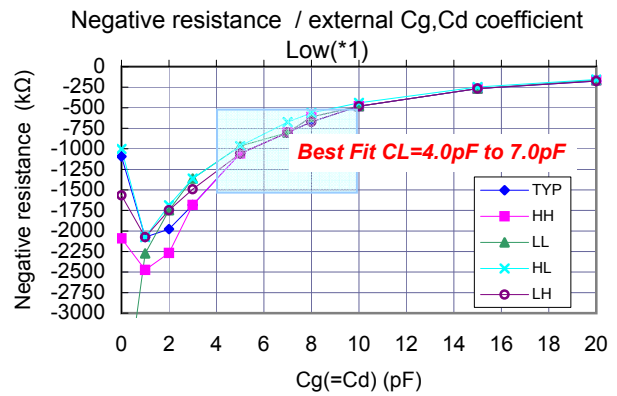
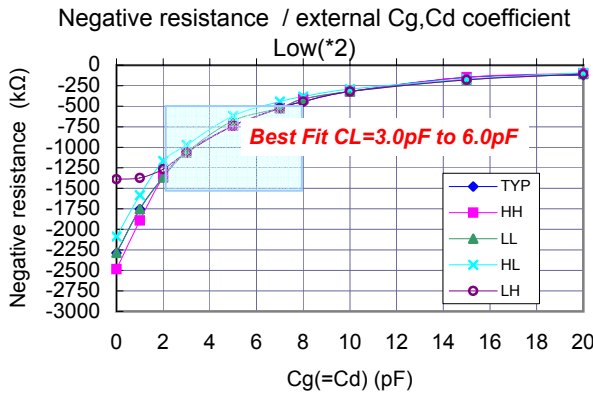
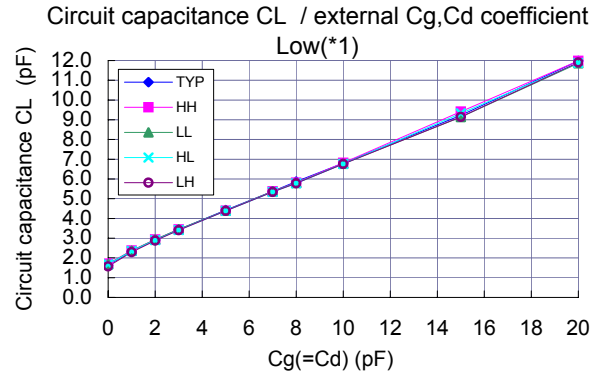
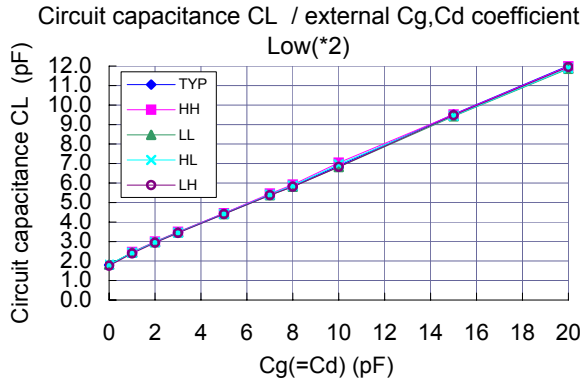
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Measurement conditions : Vdd=1.8V to 5.5V at 25°C



Referential Data(3) : External capacitance Cg,Cd characteristics



*2 ; Extremely low current consumption mode

*1 ; Low current consumption mode

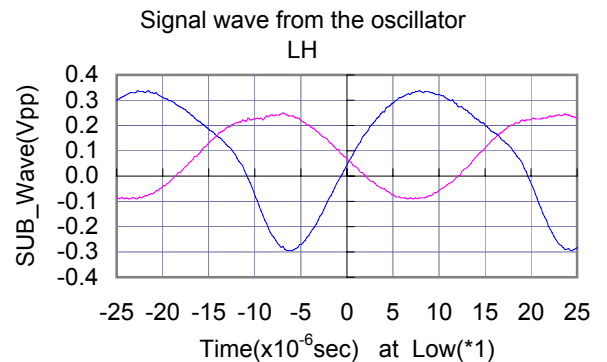
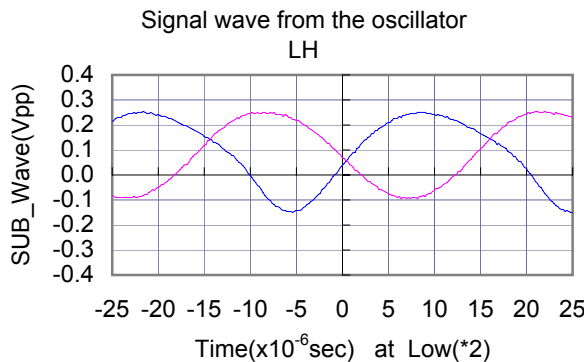
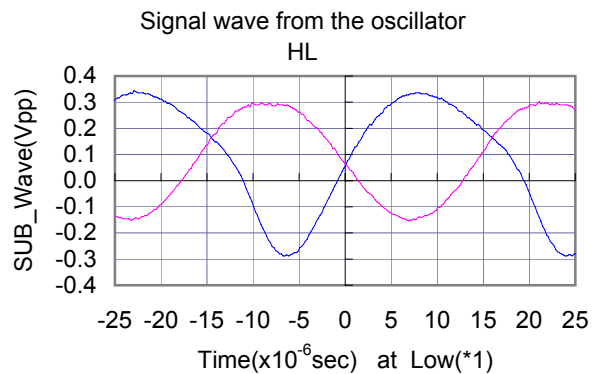
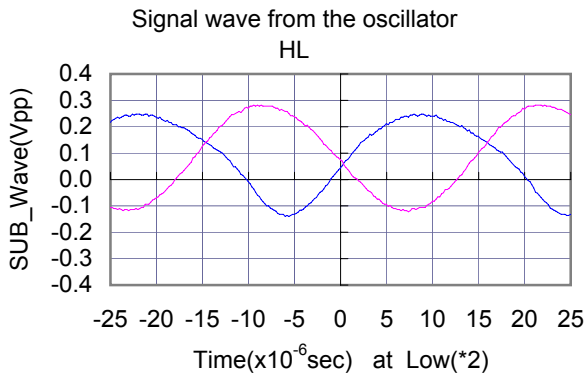
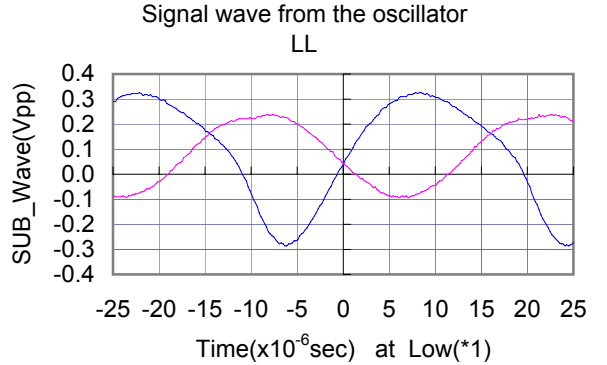
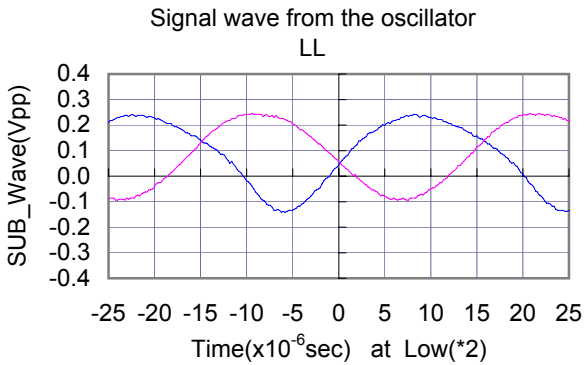
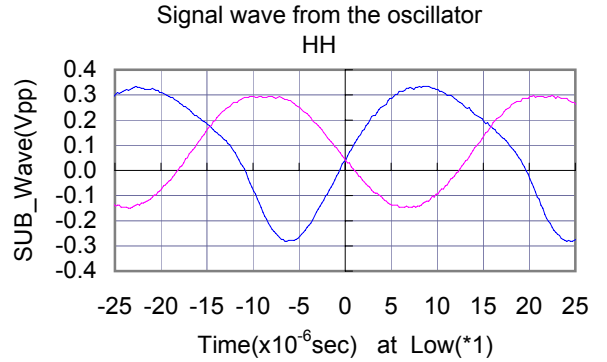
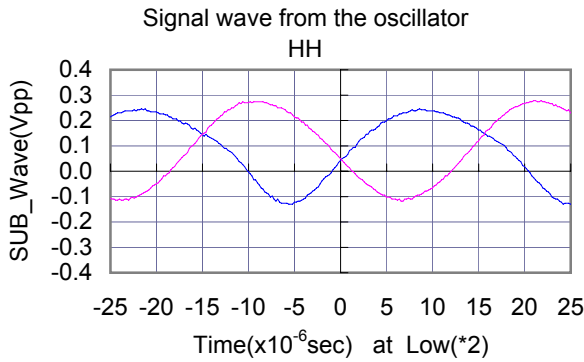
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Measurement conditions : Vdd=1.8V to 5.5V at 25°C



Referential Data(4) : Signal wave from oscillator(HH,HL,LH,LL)



**2 ; Extremely low current consumption mode*

**1 ; Low current consumption mode*

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VT-200-FL 3.7pF with uPD78F1009GB-16BT [LQFP(10x10) 0.50mm pitch]

Measurement conditions : V_{DD}=1.8V to 5.5V at 25°C

Referential Data(5) : Negative resistance (RL) & Oscillation allowance (M)_Map

Negative resistance RL(KΩ) at 25°C

TYP_Cg,Cd	Low(*2)	Low(*1)	Normal	CL(pF)
20	121	176	286	12.0
15	147	267	477	9.5
10	320	480	800	6.9
8	442	672	1052	5.8
5	737	1057	1877	4.4
2	1366	1976	2266	3.0
0	2287	1087	0	1.8

Oscillation allowance M (= RL / R_{1max}) at 25°C

TYP_Cg,Cd	Low(*2)	Low(*1)	Normal	CL(pF)
20	2	4	6	12.0
15	3	5	10	9.5
10	6	10	16	6.9
8	9	13	21	5.8
5	15	21	38	4.4
2	27	40	45	3.0
0	46	22	0	1.8

* R_{1max}=50kΩ

Negative resistance RL(KΩ) at 25°C

HH_Cg,Cd	Low(*2)	Low(*1)	Normal	CL(pF)
20	97	166	266	12.0
15	147	267	437	9.5
10	320	480	800	7.0
8	412	612	1152	5.9
5	737	1057	2057	4.4
2	1366	2266	3566	3.0
0	2485	2085	0	1.9

Oscillation allowance M (= RL / R_{1max}) at 25°C

HH_Cg,Cd	Low(*2)	Low(*1)	Normal	CL(pF)
20	2	3	5	12.0
15	3	5	9	9.5
10	6	10	16	7.0
8	8	12	23	5.9
5	15	21	41	4.4
2	27	45	71	3.0
0	50	42	0	1.9

* R_{1max}=50kΩ

Negative resistance RL(KΩ) at 25°C

LL_Cg,Cd	Low(*2)	Low(*1)	Normal	CL(pF)
20	108	166	266	11.9
15	177	267	437	9.4
10	320	480	670	6.8
8	412	612	802	5.8
5	677	967	1057	4.4
2	1366	1746	1886	3.0
0	2287	4387	0	1.8

Oscillation allowance M (= RL / R_{1max}) at 25°C

LL_Cg,Cd	Low(*2)	Low(*1)	Normal	CL(pF)
20	2	3	5	11.9
15	4	5	9	9.4
10	6	10	13	6.8
8	8	12	16	5.8
5	14	19	21	4.4
2	27	35	38	3.0
0	46	88	0	1.8

* R_{1max}=50kΩ

Negative resistance RL(KΩ) at 25°C

HL_Cg,Cd	Low(*2)	Low(*1)	Normal	CL(pF)
20	93	156	246	11.9
15	167	247	407	9.4
10	290	440	730	7.0
8	382	562	962	5.9
5	617	967	1487	4.4
2	1166	1686	2666	3.0
0	2087	997	0	1.8

Oscillation allowance M (= RL / R_{1max}) at 25°C

HL_Cg,Cd	Low(*2)	Low(*1)	Normal	CL(pF)
20	2	3	5	11.9
15	3	5	8	9.4
10	6	9	15	7.0
8	8	11	19	5.9
5	12	19	30	4.4
2	23	34	53	3.0
0	42	20	0	1.8

* R_{1max}=50kΩ

Negative resistance RL(KΩ) at 25°C

LH_Cg,Cd	Low(*2)	Low(*1)	Normal	CL(pF)
20	108	176	286	12.0
15	177	267	477	9.5
10	320	480	800	6.8
8	442	672	1052	5.8
5	737	1057	1567	4.4
2	1267	1747	2667	2.9
0	1388	1558	0	1.8

Oscillation allowance M (= RL / R_{1max}) at 25°C

LH_Cg,Cd	Low(*2)	Low(*1)	Normal	CL(pF)
20	2	4	6	12.0
15	4	5	10	9.5
10	6	10	16	6.8
8	9	13	21	5.8
5	15	21	31	4.4
2	25	35	53	2.9
0	28	31	0	1.8

* R_{1max}=50kΩ

Evaluation of a Low Frequency Clock Oscillation Circuit

VT-200-FL 3.7pF with uPD78F1009GB-16BT [LQFP(10x10) 0.50mm pitch]

Measurement conditions : Vdd=1.8V to 5.5V



Referential Data(6) : Circuit characteristics (TYP,HH,LL) at -40°C / +85°C

at -40°C

Circuit characteristics (TYP)	Low(*2)	Low(*1)
Negative resistance : - RL (kΩ)	810	1060
Oscillation allowance: M(times)	16	21
Oscillation start up time: Ts(sec)	0.92	0.60

*1; Low current consumption mode (M=27 at 25°C)
*2; Extremely low current consumption mode (M=19 at 25°C)

at 85°C

Circuit characteristics (TYP)	Low(*2)	Low(*1)
Negative resistance : - RL (kΩ)	1060	1360
Oscillation allowance: M(times)	21	27
Oscillation start up time: Ts(sec)	0.57	0.45

*1; Low current consumption mode (M=27 at 25°C)
*2; Extremely low current consumption mode (M=19 at 25°C)

at -40°C

Circuit characteristics (HH)	Low(*2)	Low(*1)
Negative resistance : - RL (kΩ)	810	1160
Oscillation allowance: M(times)	16	23
Oscillation start up time: Ts(sec)	1.24	0.75

*1; Low current consumption mode (M=27 at 25°C)
*2; Extremely low current consumption mode (M=19 at 25°C)

at 85°C

Circuit characteristics (HH)	Low(*2)	Low(*1)
Negative resistance : - RL (kΩ)	1060	1880
Oscillation allowance: M(times)	21	38
Oscillation start up time: Ts(sec)	0.58	0.45

*1; Low current consumption mode (M=27 at 25°C)
*2; Extremely low current consumption mode (M=19 at 25°C)

at -40°C

Circuit characteristics (LL)	Low(*2)	Low(*1)
Negative resistance : - RL (kΩ)	740	970
Oscillation allowance: M(times)	15	19
Oscillation start up time: Ts(sec)	1.01	0.61

*1; Low current consumption mode (M=25 at 25°C)
*2; Extremely low current consumption mode (M=19 at 25°C)

at 85°C

Circuit characteristics (LL)	Low(*2)	Low(*1)
Negative resistance : - RL (kΩ)	970	1260
Oscillation allowance: M(times)	19	25
Oscillation start up time: Ts(sec)	0.65	0.51

*1; Low current consumption mode (M=25 at 25°C)
*2; Extremely low current consumption mode (M=19 at 25°C)

Extremely low power consumption of 1/10 : 78K0R/Kx3-L & Low CL series

* It is achieved by the technical collaboration to make low AMP and low CL Tuning Fork.

NEC MPU 78K0R/Kx3-L series

78K0R/KC3-L;uPD78F1000MC/1001MC/1002MC/1003MC
uPD78F1000GA/1001GA/1002GA/1003GA
uPD78F1000GB/1001GB/1002GB/1003GB
78K0R/KD3-L;uPDF1004GB/1005GB/1006GB
78K0R/KE3-L;uPD78F1007GA/1008GA/1009GA
uPD78F1007GB/1008GB/1009GB
uPD78F1007GK/1008GK/1009GK

Normal current consumption <500nA

