

Evaluation of a Low Frequency Clock Oscillation Circuit

VT-200-FL 4.4pF with R5F2L36CANFP-64P [LQFP(10x10) 0.50mm pitch]

Measurement conditions : 3.3V ,5.0V



New

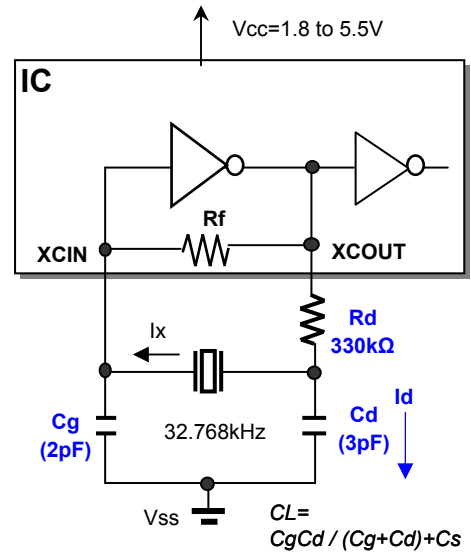
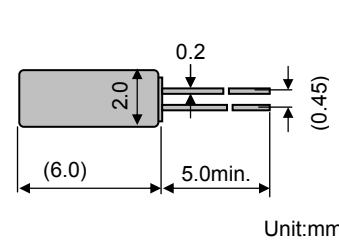


Model	:VT-200-FL
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10 ⁻⁶
Load capacitance	:CL=4.4pF
Equivalent series resistance	:R1=50kΩ max
Max. drive level	:DL=1μW max
Level of drive	:DL=0.01μW typ

FEATURES

- 1.Compact tubular package
- 2.Photolithographic process
- 3.Excellent shock resistance and environmental characteristics.
- 4.Real time clocks, Timers, Portable applications

DIMENSIONS(VT-200)



Remark) Ix : current through crystal

Super low power consumption R8C/Lx and VT-200-FL 4.4pF

Resonators for small load capacitance are best fitted for super low power oscillation. Utmost performance to fulfill your expectations has been realized.

MODEL:VT-200-FL 4.4pF with R5F2L36CANFP at 25°C

Key specifications	Vcc=3.3V	Vcc=5.0V	Remarks
Current control resistance : Rd (kΩ)	330	330	Control drive level & secure phase margin
Capacitance at gate : Cg (pF)	2	2	Optimal capacitance in response to CL
Capacitance at drain : Cd (pF)	3	3	(CL = Cd // Cg + stray capacitance)

Circuit characteristics (at 25°C)	Vcc=3.3V	Vcc=5.0V	Remarks
Matching Accuracy : df / f (x10 ⁻⁶)	1.6	3.5	Frequency offset volume at specified Vcc
Voltage Fluctuation : +/-df / V (x10 ⁻⁶)	0.3	0.9	Vcc +/-10% (Standard operating voltage range)
Drive Level : DL (μW)	0.012	0.016	DL=Ix ² Re < 1x10 ⁻⁶ W, Re=R1(1 + Co / CL) ²
Negative resistance : - RL (kΩ)	1159	1359	5 times larger than R _{1MAX}
Oscillation allowance : M (times)	23	27	Judgmental standard of oscillation stability
Super low current consumption : Id (nA)	121	139	Cd charge current, Id = ωCd*Vd < 150nA
Voltage of oscillation start : Vstart (V)	1.23	1.23	
Voltage of oscillation stop : Vstop (V)	1.21	1.21	
Oscillation start up time : Ts (sec)	0.38	0.31	Time to reach 90% of output level, Ts < 0.6sec

Temperature characteristics of circuit		Vcc=3.3V	Vcc=5.0V	Remarks
at -40°C	Variation : df / T (x10 ⁻⁶)	-138	-138	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)
at +85°C	Variation : df / T (x10 ⁻⁶)	-135	-135	Typ.Tp=25°C (K = -3.5x10 ⁻⁸ / °C ²)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

Seiko Instruments USA Inc.

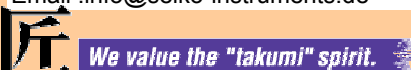
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Evaluation of a Low Frequency Clock Oscillation Circuit

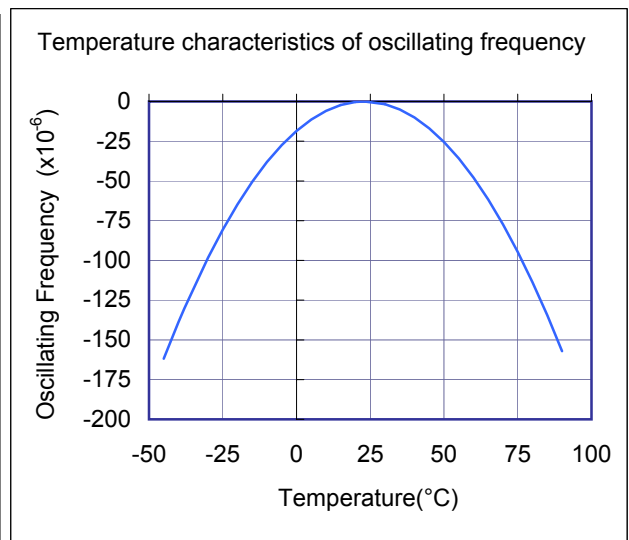
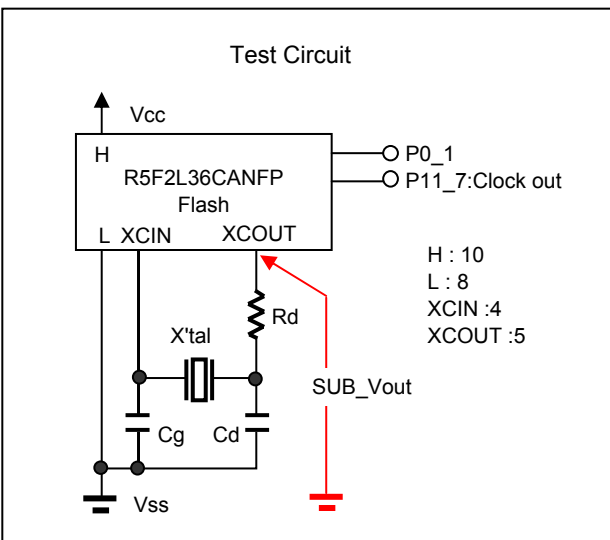
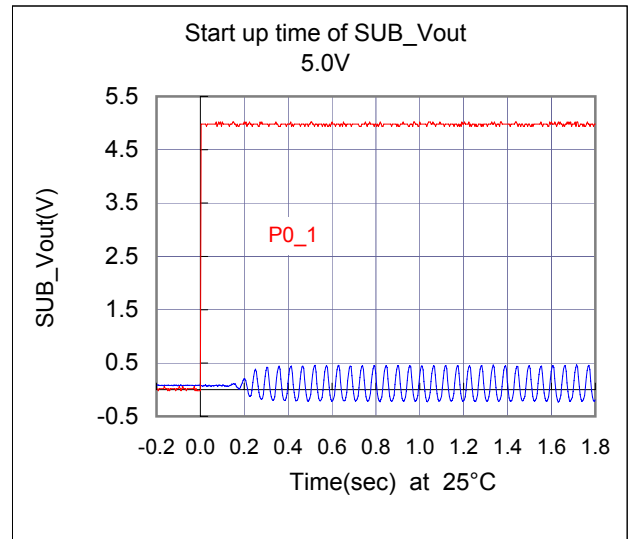
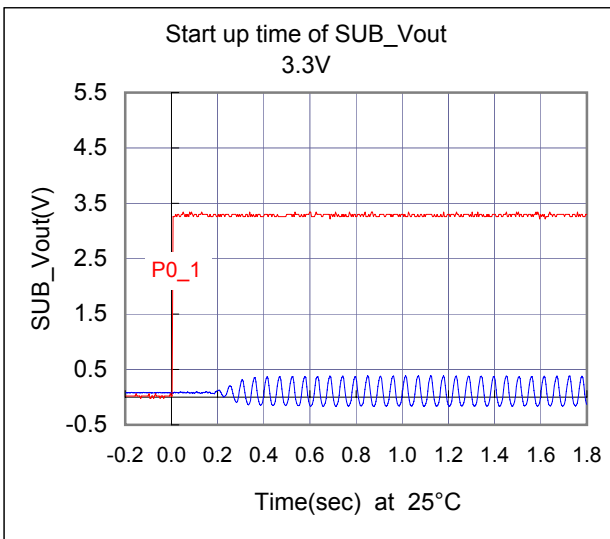
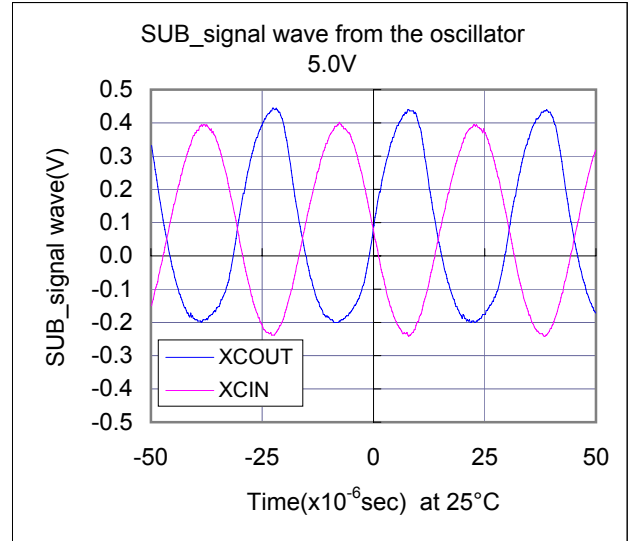
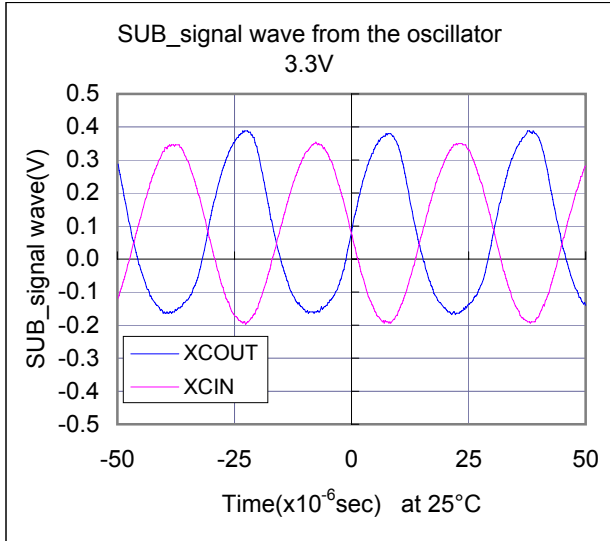
VT-200-FL 4.4pF with R5F2L36CANFP-64P [LQFP(10x10) 0.50mm pitch]

Measurement conditions : 3.3V ,5.0V



Super low power consumption MPU

Test Data



Evaluation of a Low Frequency Clock Oscillation Circuit

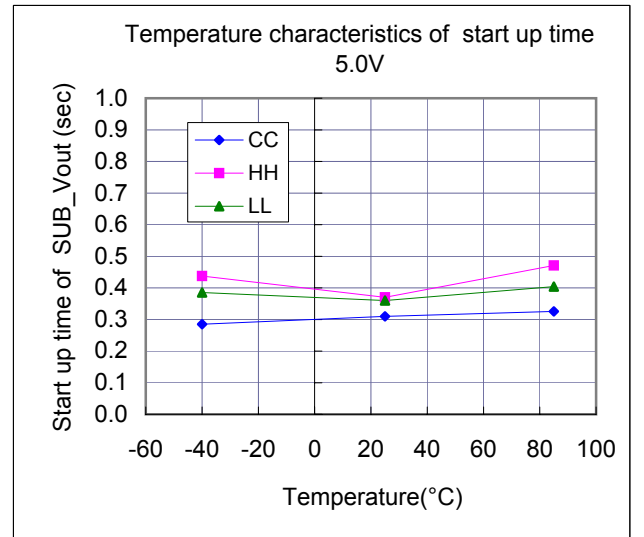
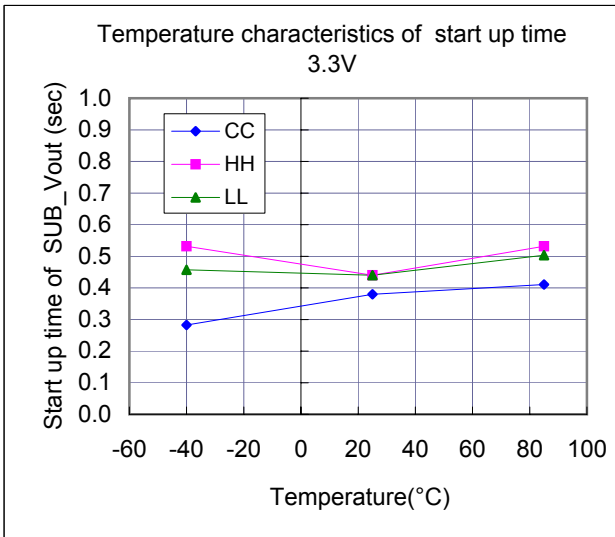
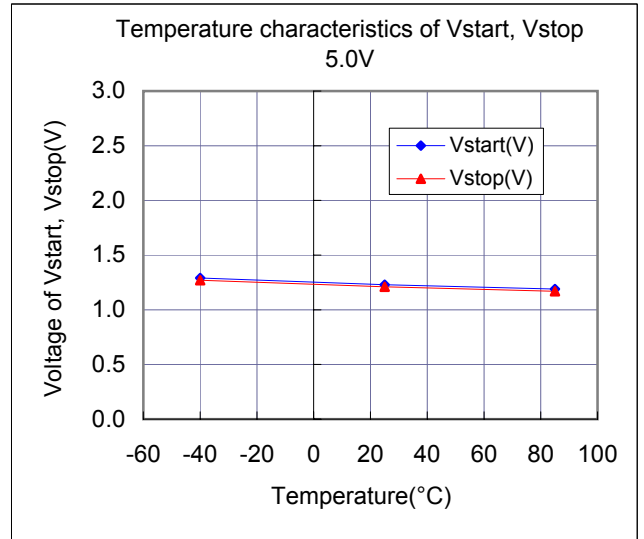
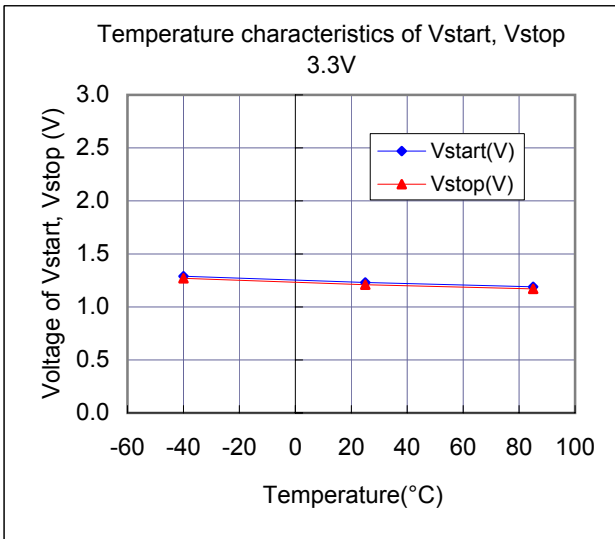
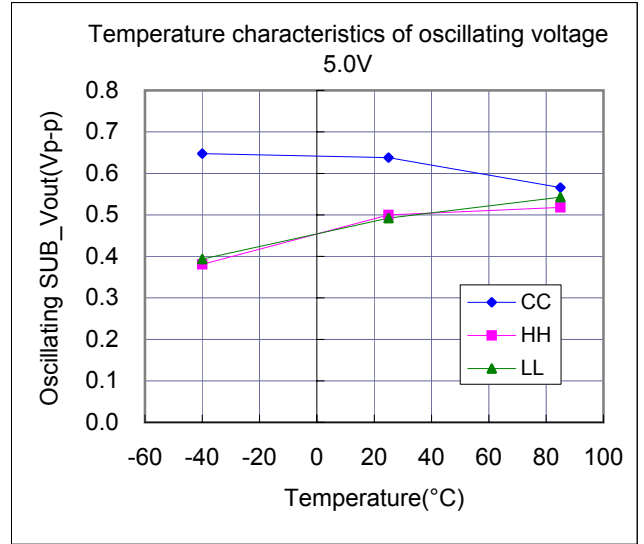
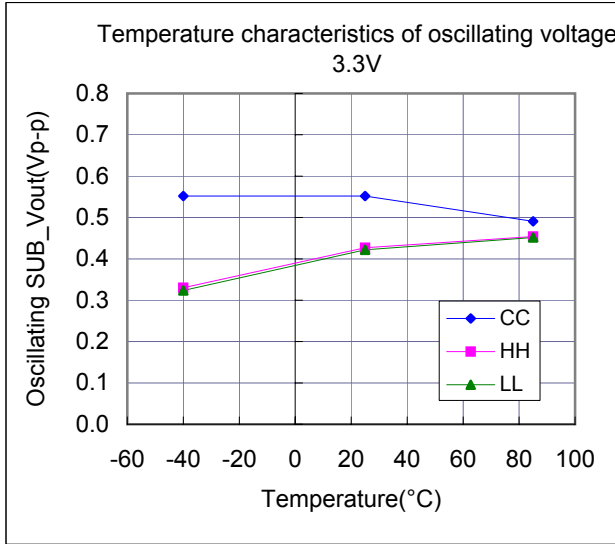
VT-200-FL 4.4pF with R5F2L36CANFP-64P [LQFP(10x10) 0.50mm pitch]

Measurement conditions : 3.3V ,5.0V



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Test Data : Temperature characteristics(CC,HH,LL)



Evaluation of a Low Frequency Clock Oscillation Circuit

VT-200-FL 4.4pF with R5F2L36CANFP-64P [LQFP(10x10) 0.50mm pitch]

Measurement conditions : 3.3V ,5.0V



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Referential components layout(see Figure 1)

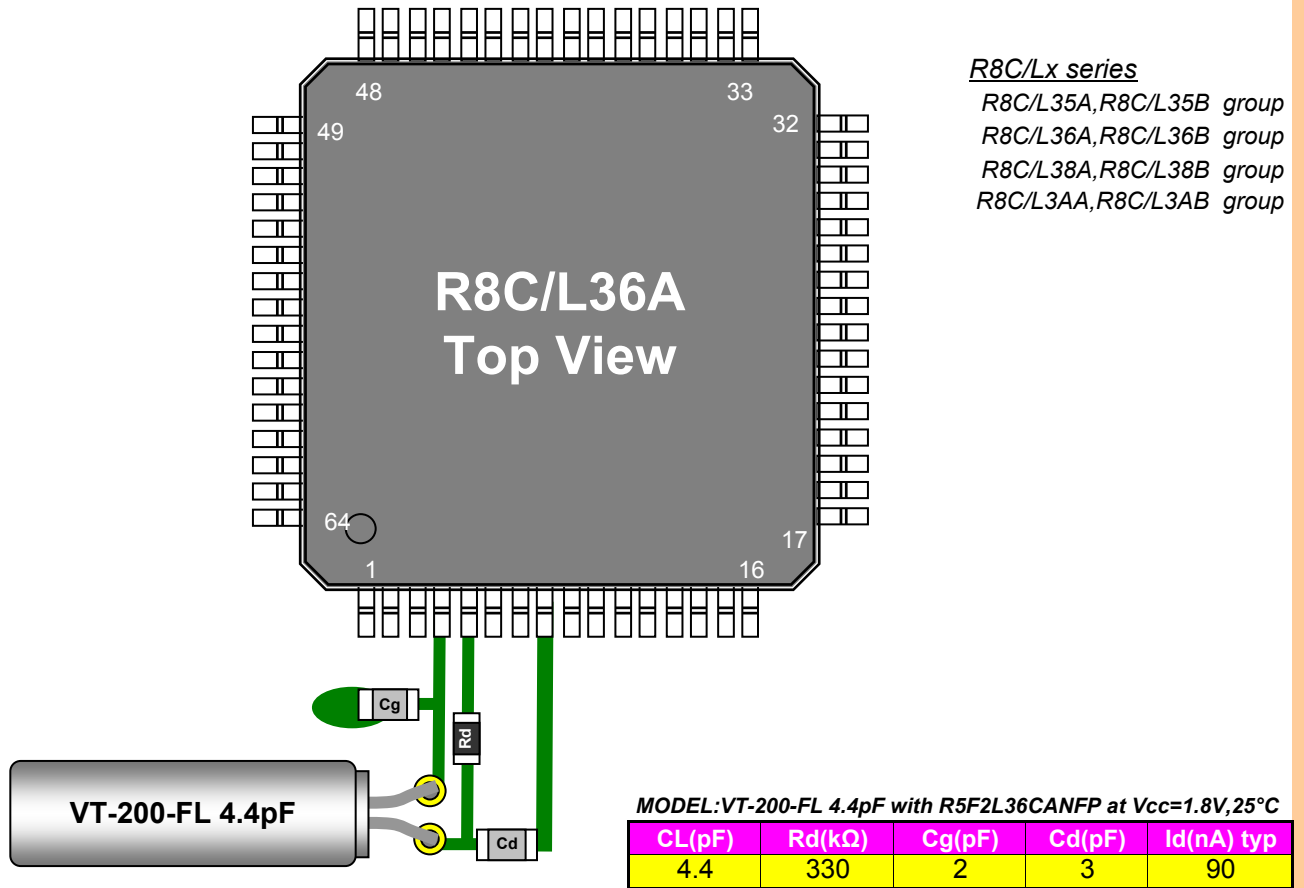


Figure 1 Referential components layout

Notes Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

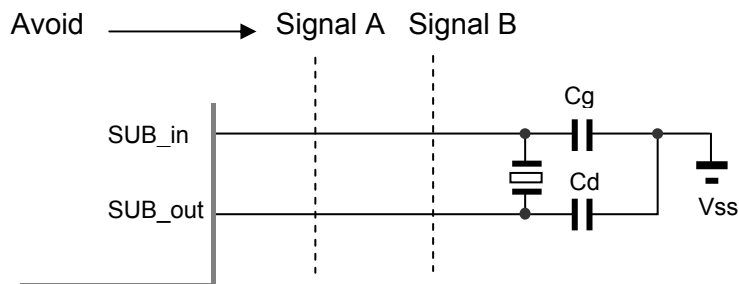


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert a resistor, Rd, in series on the SUB_out side.

Evaluation of a Low Frequency Clock Oscillation Circuit

VT-200-FL 4.4pF with R5F2L36CANFP-64P [LQFP(10x10) 0.50mm pitch]

Measurement conditions : 3.3V ,5.0V



Super low power consumption MPU

[Evaluation Sample at 25°C]

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kΩ)	Co(pF)	C1(fF)	Q(k)
VT-200-FL	1	4.4	32767.96	32761.56	38.1	0.89	2.066	61.8
	2	4.4	32768.04	32761.58	40.0	0.90	2.090	58.1
	3	4.4	32768.04	32761.59	39.8	0.90	2.086	58.5

[IC Test Data : IC Sample Rd=330kΩ,Cg=2pF,Cd=3pF at 25°C]

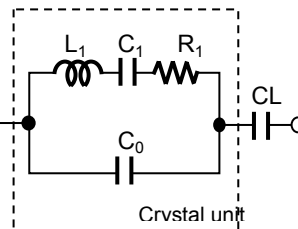
Vcc(V)	IC Sample	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(μW)	-RL (kΩ)	Id (nA)	DC_Bias(V)	Vstart(V)	Ts(sec)
5.0	CC	32768.16	3.5	0.016	1359	139	0.94	1.23	0.31
	HH	32768.00	-1.2	0.011	1059	110	0.73	1.30	0.37
	HL	32768.04	0.0	0.008	1059	99	0.72	1.32	0.36
	LH	32768.14	3.1	0.012	1059	122	0.76	1.22	0.42
	LL	32768.15	3.3	0.010	1059	107	0.65	1.28	0.42

[IC Test Data : IC Sample Rd=330kΩ,Cg=2pF,Cd=3pF at 25°C]

Vcc(V)	IC Sample	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(μW)	-RL (kΩ)	Id (nA)	DC_Bias(V)	Vstart(V)	Ts(sec)
3.3	CC	32768.09	1.6	0.012	1159	121	0.87	1.23	0.38
	HH	32767.93	-3.4	0.008	909	93	0.65	1.30	0.44
	HL	32767.96	-2.4	0.006	909	82	0.64	1.32	0.44
	LH	32768.06	0.7	0.009	909	102	0.68	1.22	0.47
	LL	32768.06	0.7	0.007	909	92	0.57	1.28	0.47

Remark (see figure 3)

$$F_o = f_r \times \left\{ \frac{C_1}{2 \times (C_o + C_L)} + 1 \right\} \text{ (Hz)}$$



Fo : Load resonance frequency
fr : Resonance frequency
R1 : Motional resistance
C1 : Motional capacitance
Co : Shunt capacitance
CL : Load Capacitance

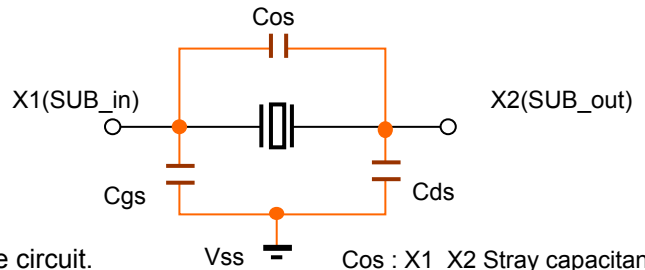
Figure 3 Equivalent circuit of crystal unit, and CL**Remark (see figure 4)**

Approximate formula of the load capacitance of the circuit CL,

$$C_L = C_g \times C_d / (C_g + C_d) + C_s \text{ (pF)}$$

$$C_s = C_{gs} \times C_{ds} / (C_{gs} + C_{ds}) + C_{os} \text{ (pF)}$$

where Cs(=3 to 5pF) stands for stray capacitance of the circuit.



Cos : X1_X2 Stray capacitance
Cgs : X1_Vss Stray capacitance
Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.



Evaluation of a Low Frequency Clock Oscillation Circuit

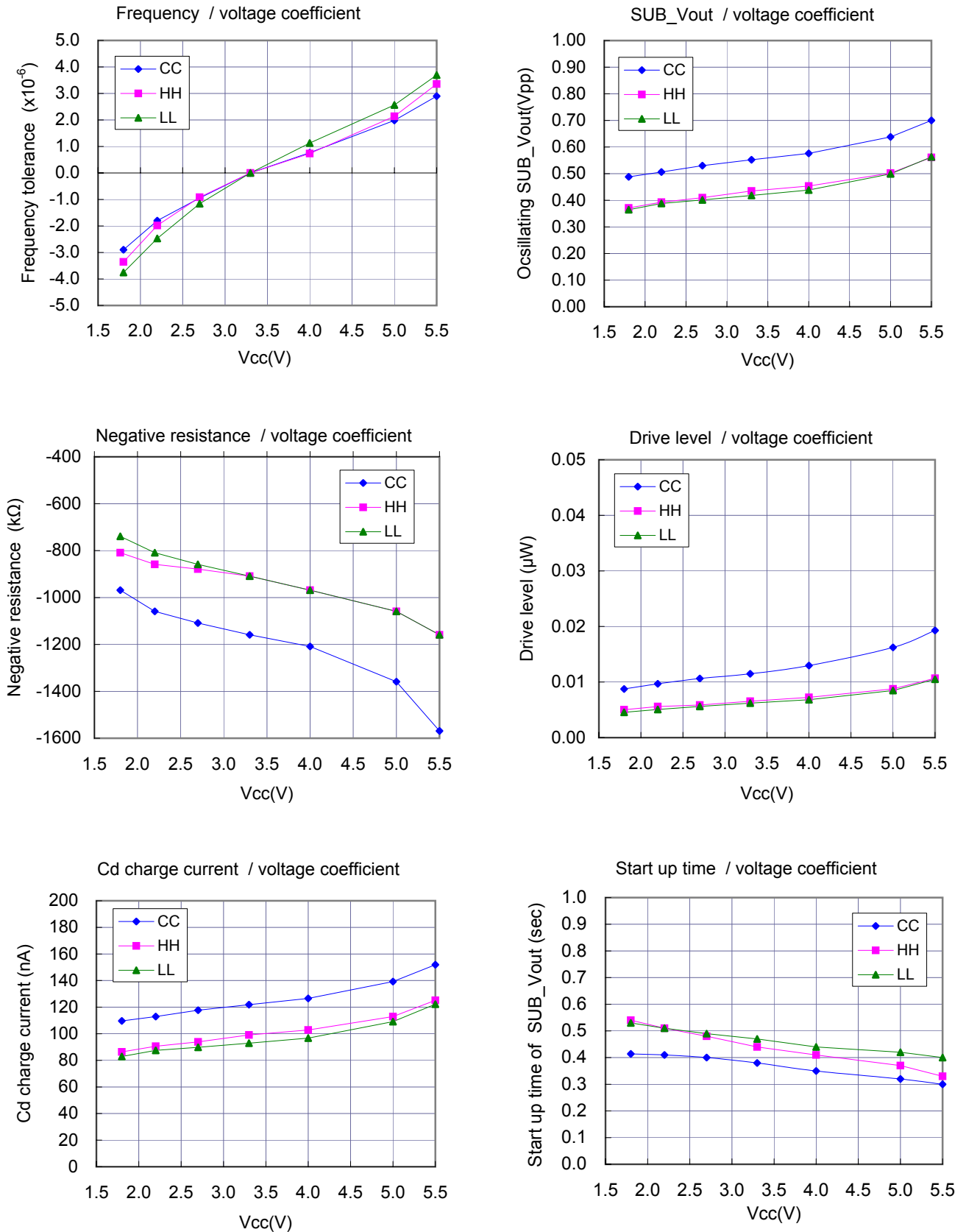
VT-200-FL 4.4pF with R5F2L36CANFP-64P [LQFP(10x10) 0.50mm pitch]

Measurement conditions : Vcc=1.8V to 5.5V at 25°C



Super low power consumption MPU

Referential Data(1): Voltage characteristics (CC,HH,LL)



Evaluation of a Low Frequency Clock Oscillation Circuit

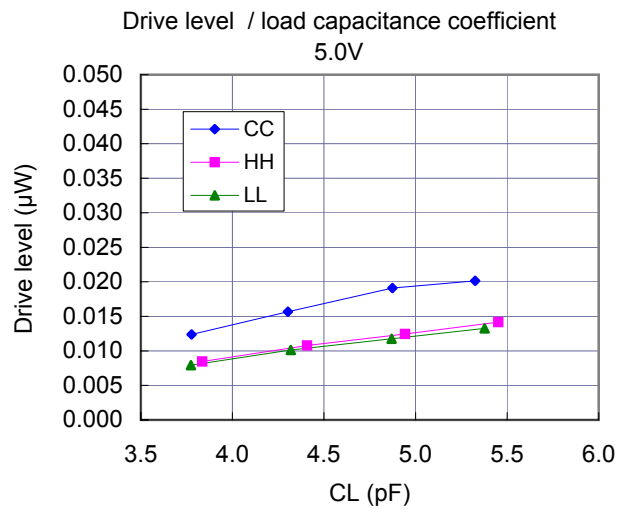
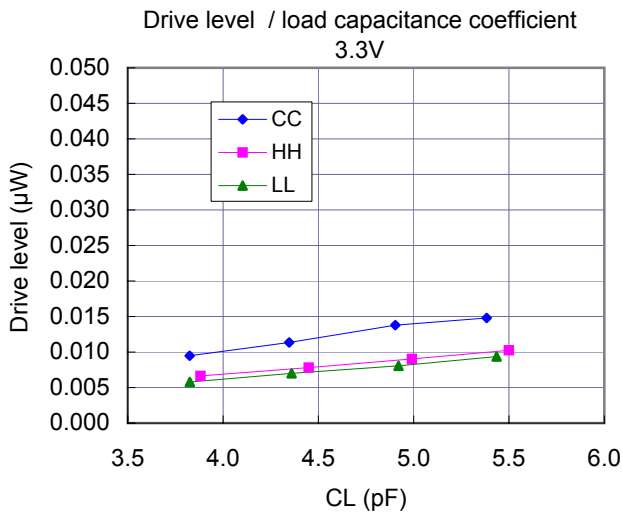
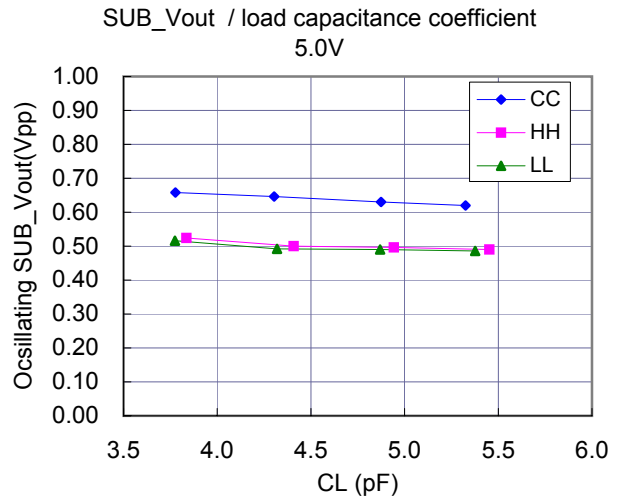
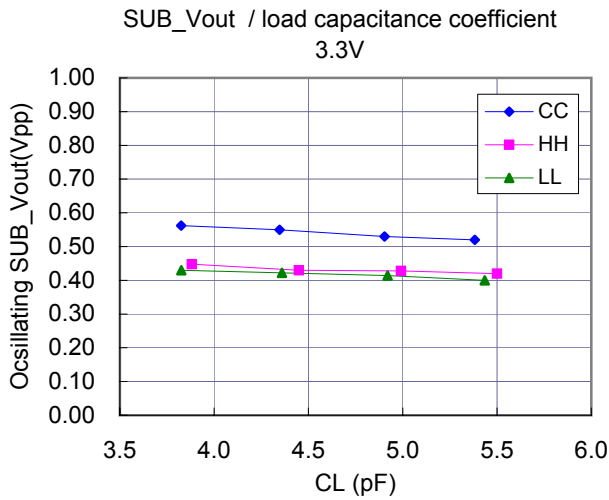
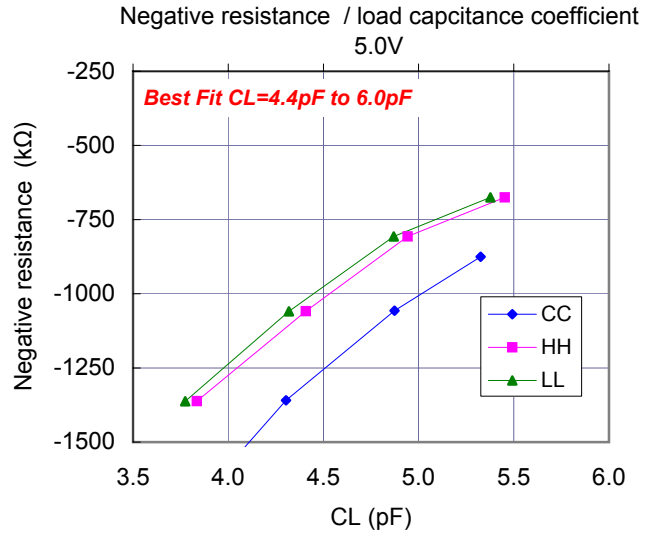
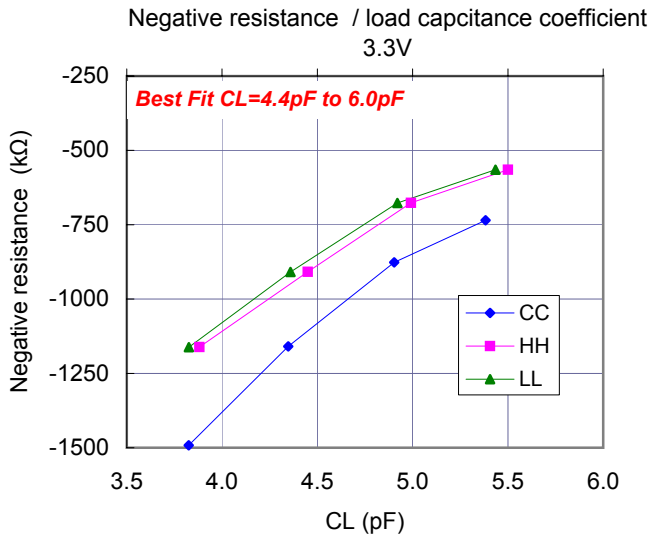
VT-200-FL 4.4pF with R5F2L36CANFP-64P [LQFP(10x10) 0.50mm pitch]

Measurement conditions : Vdd=3.3V,5.0V at 25°C



Super low power consumption MPU

Referential Data(2) : Load capacitance characteristics(CC,HH,LL)



Evaluation of a Low Frequency Clock Oscillation Circuit

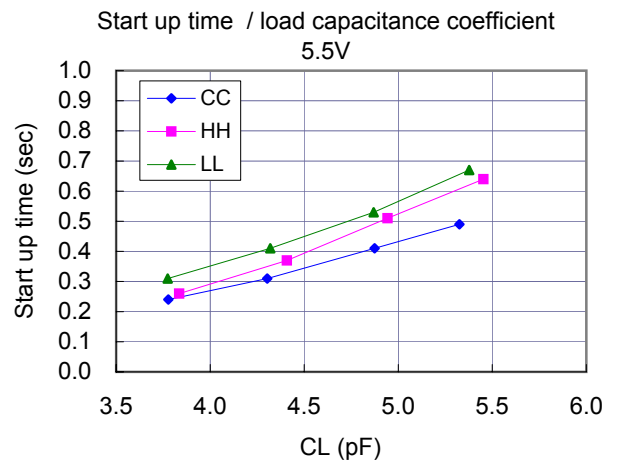
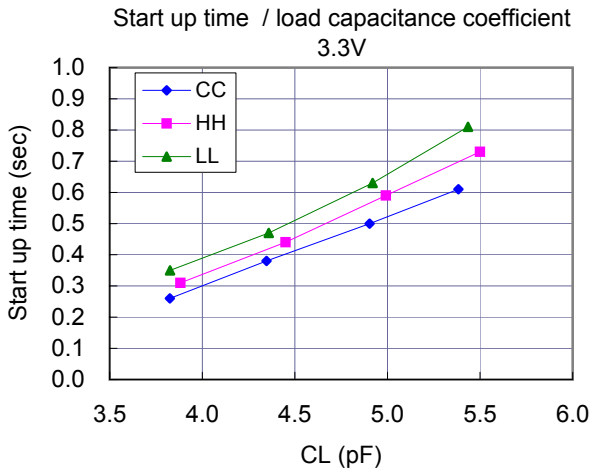
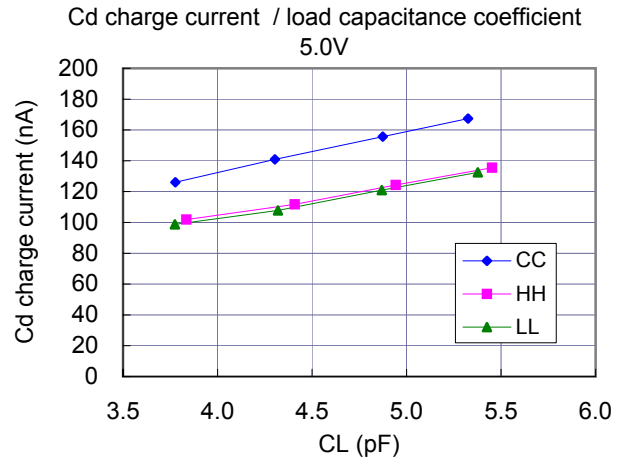
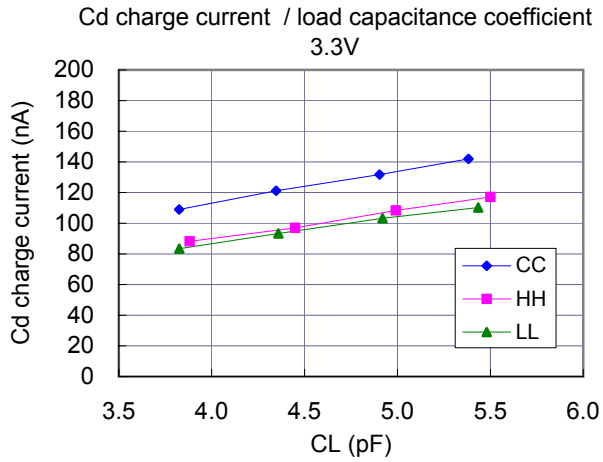
VT-200-FL 4.4pF with R5F2L36CANFP-64P [LQFP(10x10) 0.50mm pitch]

Measurement conditions : Vdd=3.3V,5.0V at 25°C



Super low power consumption MPU

Referential Data(3) : Load capacitance characteristics(CC,HH,LL)



Super low power consumption R8C/Lx and Low CL VT-200-FL 4.4pF

The R8C/Lx series are a range of super low power consumption microcontrollers, fitting the needs of power reduction at stand-by mode for longer battery life.



Table 1 XCIN oscillation circuit and load capacitance for a resonator

CL(pF)	Rd(kΩ)	Cg(pF)	Cg(pF)	Vcc (Cd charge current: Id)
6.0	0	5	5	3.3V(180nA typ),5.0V(210nA typ)
4.4	330	2	3	3.3V(100nA typ),5.0V(115nA typ)

*RENESAS MPU R8C/Lx group; R8C/L35x,R8C/L36x,R8C/L38x and R8C/L3Ax & VT-200 series

IC sample Rd=0Ω,Cg=5pF,Cd=5pF,CL=6.0pF

IC sample Rd=330kΩ,Cg=2pF,Cd=3F,CL=4.4pF

Vcc(V)	IC sample	M(times) [*]	Id(nA)	Ts(sec)	Vcc(V)	IC sample	M(times) [*]	Id(nA)	Ts(sec)
5.0	CC	21	252	0.59	5.0	CC	27	139	0.31
	HH	15	203	0.67		HH	21	110	0.37
	HL	16	176	0.67		HL	21	99	0.36
	LH	16	222	0.72		LH	21	122	0.42
	LL	16	203	0.73		LL	21	107	0.42
3.3	CC	18	219	0.67	3.3	CC	23	121	0.38
	HH	13	177	0.77		HH	18	93	0.44
	HL	13	149	0.75		HL	18	82	0.44
	LH	13	193	0.78		LH	18	102	0.47
	LL	13	175	0.77		LL	18	92	0.47

*R1max=50kΩ

*R1max=50kΩ



Evaluation of a Low Frequency Clock Oscillation Circuit

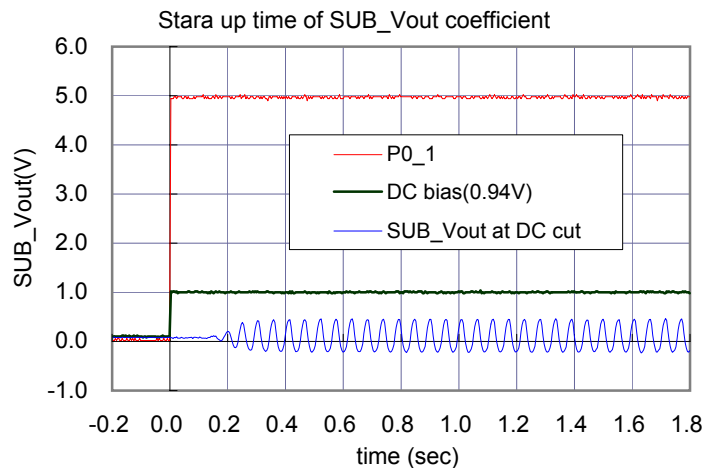
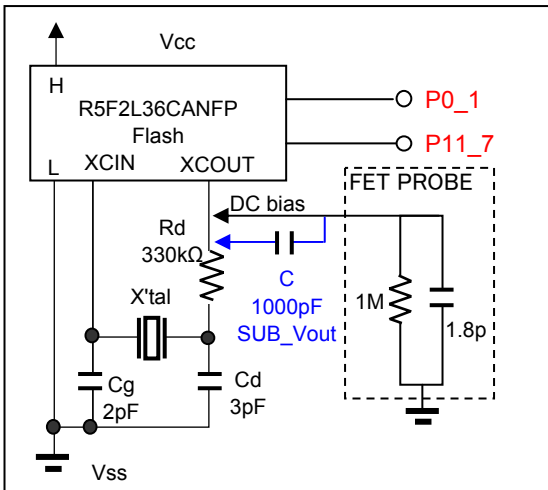
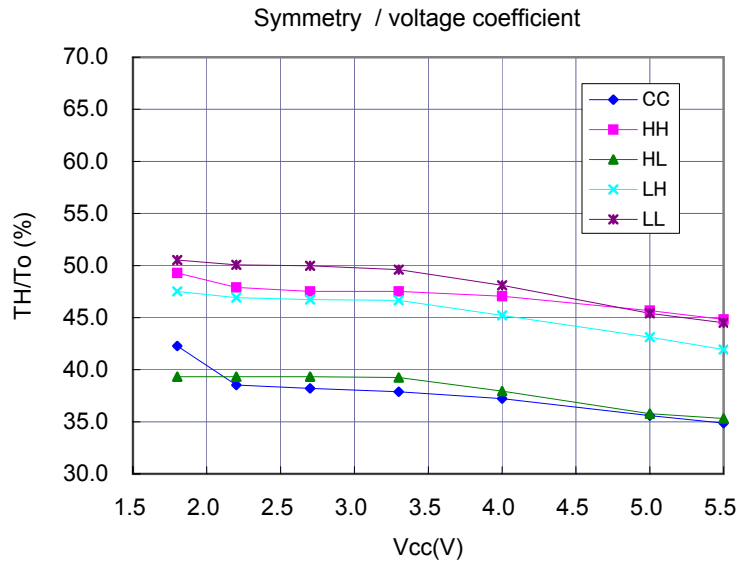
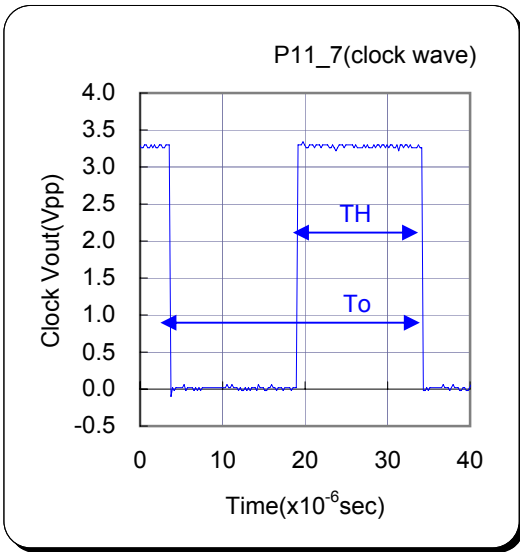
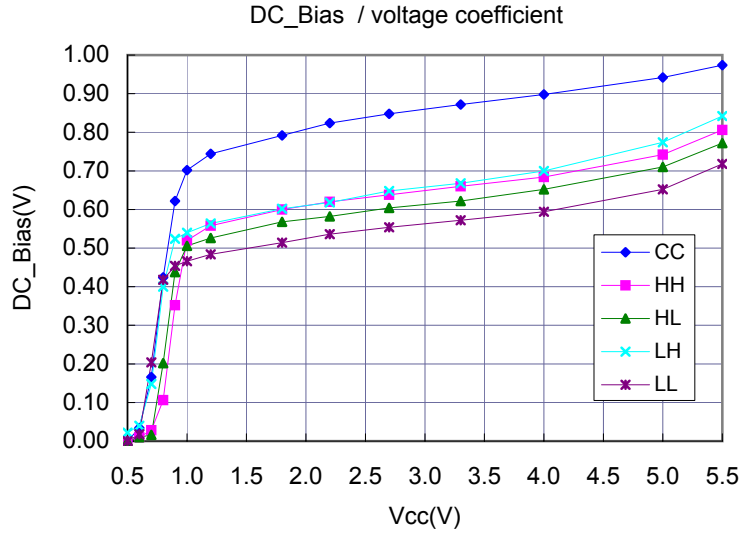
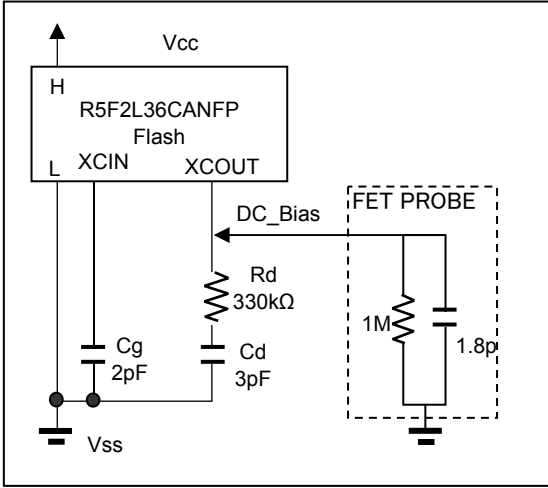
VT-200-FL 4.4pF with R5F2L36CANFP-64P [LQFP(10x10) 0.50mm pitch]

Measurement conditions : Vcc=(0.5V) to 5.5V at 25°C



Super low power consumption MPU

Referential Data(4) : BC_Bias and Symmetry characteristics(CC,HH,HL,LH,LL)



Evaluation of a Low Frequency Clock Oscillation Circuit

VT-200-FL 4.4pF with R5F2L36CANFP-64P [LQFP(10x10) 0.50mm pitch]

Measurement conditions : Vdd=3.3V,5.0V at 25°C



Super low power consumption MPU

Referential Data(6) : Selection of XCIN oscillation mode and recommended load capacitance

For R8C/Lx series

XCIN oscillation circuit consists of an excellent power saving circuit which realizes stable oscillation at low amplitude.

RENESAS MPU R8C/Lx series

- R8C/L35A group, R8C/L35B group (52pin)
- R8C/L36A group, R8C/L36B group (64pin)
- R8C/L38A group, R8C/L38B group (80pin)
- R8C/L3AA group, R8C/L3AB group (100pin)

For your design reliability, please refer to Table 1 which shows the performance of the XCIN oscillation circuit and the recommended load capacitance for each resonator.

VT-200 series

VT-200-FL CL=3.7pF,4.4pF,6.0pF and VT-200-F CL=8.7pF

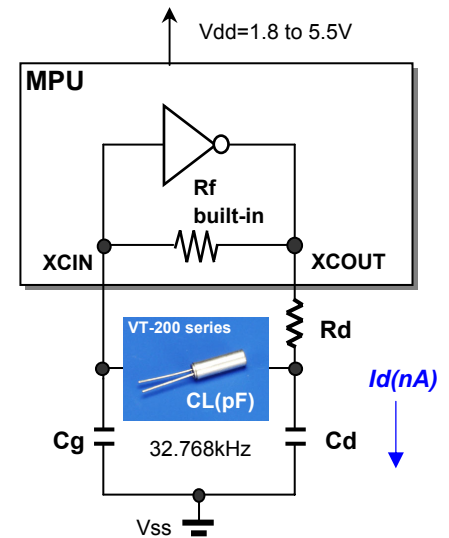
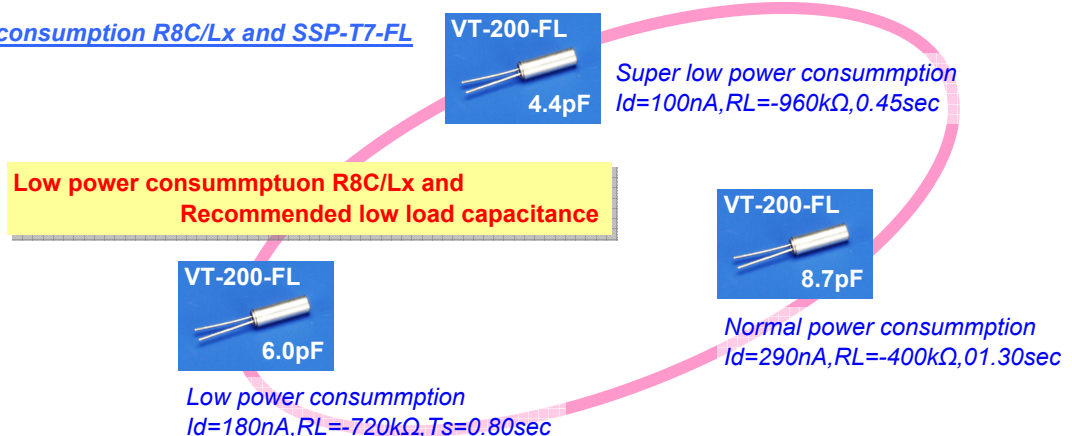


Table 1 XCIN oscillation circuit and load capacitance for a resonator

Resonator	Vcc	Recommended circuit constant and load capacitance for a resonator			
		Rd=330kΩ Cg=2pF,Cd=3pF	Rd=0Ω Cg=5pF,Cd=5pF	Rd=0Ω Cg=7pF,Cd=7pF	Rd=0Ω Cg=10pF,Cd=10pF
VT-200-FL Low CL resonator	5.0V	VT-200-FL 4.4pF <i>Id=115nA typ</i> <i>RL=-1120kΩ typ</i> <i>Ts=0.40sec typ</i>	VT-200-FL 6.0pF <i>Id=210nA typ</i> <i>RL=-840kΩ typ</i> <i>Ts=0.70sec typ</i>	-	-
	3.3V	VT-200-FL 4.4pF <i>Id=100nA typ</i> <i>RL=-960kΩ typ</i> <i>Ts=0.45sec typ</i>	VT-200-FL 6.0pF <i>Id=180nA typ</i> <i>RL=-720kΩ typ</i> <i>Ts=0.75sec typ</i>	-	-
VT-200-F Existing product	5.0V	-	-	-	VT-200-F 8.7pF <i>Id=290nA typ</i> <i>RL=-400kΩ typ</i> <i>Ts=1.30sec typ</i>
	3.3V	-	-	-	VT-200-F 9.0pF <i>Id=245nA typ</i> <i>RL=-340kΩ typ</i> <i>Ts=1.40sec typ</i>

Super low power consumption R8C/Lx and SSP-T7-FL



Reference (Preliminary)

For R8C/Lx Series

Low CL resonator (VT-200-FL) R8C/35x,R8C/36x,R8C/38x and R8C/3Ax group



VT-200-FL 4.4pF resonator realizes super low power consumption

XCIN Oscillation Circuit (32.768kHz)

Design Support Manual

Contents

(Super low power consumption oscillation and low CL resonator)

1. Design points to remember
2. XCIN oscillation circuit and recommended load capacitance
3. Value tolerance of external capacitors and frequency stability
4. Combination with stray capacitance which minimizes maximum tolerance (examples for actual use)

Circuit Technology Section
Quartz Crystal Development Department
Seiko Instruments Inc.

1. Design points to remember

XCIN oscillation circuit is of the low amplification type in order to realize low power consumption. Please pay attention to the following points in design.
An incorrect example is shown in Figure 5.

- (1) Do not set up Signal Line A from XCIN terminal.
 - (2) Do not set up Signal Line B from XCOOUT terminal.
 - (3) Do not connect an external resistor, Rfext, between XCIN and XOUT.
- Rfext used in parallel makes the combined resistance critically small because Rf (>10MΩ) has been integrated in MPU.*

Please remember that new set-ups of signal lines or an external resistor would give negative impact on active impedance of the oscillation circuit and cause abnormal frequency and unusual oscillation behavior.

Active impedance, Zi, includes an amplifier between XCIN and XCOOUT terminals of the oscillation circuit.

Zi can be found from the analysis model of active impedance shown in Figure 6.

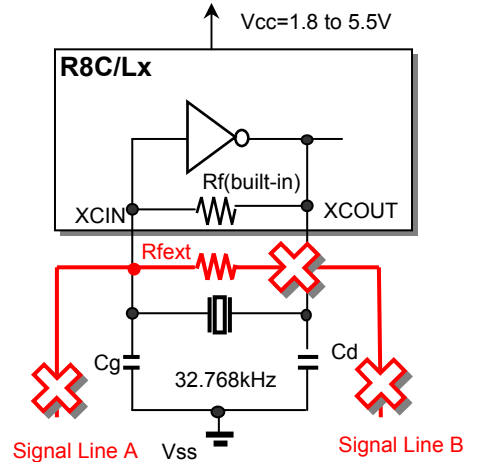


Figure 5 Incorrect example of connections in the oscillation circuit

$$Z_i = \frac{R_f \times Z_o}{R_f + Z_o} \quad (\Omega)$$

$$Z_o = g_m Z_g Z_d + (Z_g + Z_d) \quad (\Omega)$$

$$Z_g = 1 / j2\pi f C_g, \quad Z_d = 1 / j2\pi f C_d$$

$$g_m = (W/L) \mu C_{ox} (V_g - V_{Th}) \quad (\mu A/V)$$

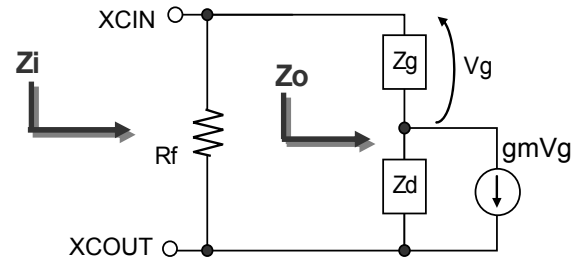


Figure 6 Example of active impedance analysis model

Making the feedback resistance, Rf(Ω), smaller than necessary would have negative impact on Zo(Ω) directly.

Incorrect examples are shown in Figure 7 and 8 when an external resistor, Rfext, is used.

The smaller Rfext value makes frequency and negative resistance deviate from Zo characteristics' track significantly, which causes abnormal frequency and unusual oscillation behavior. Take care in design.

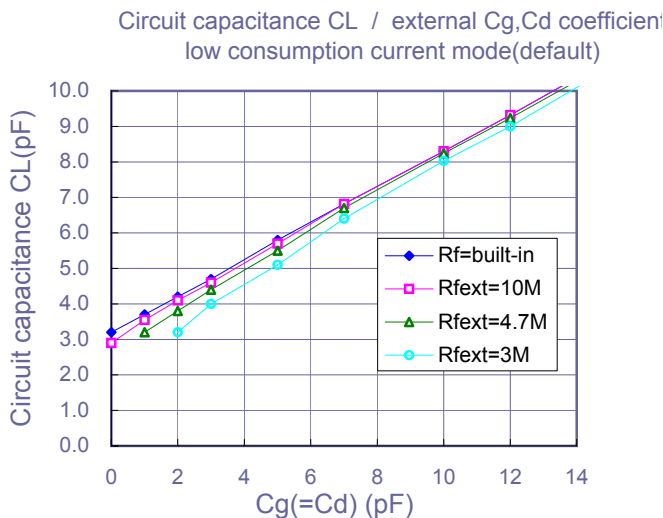


Figure 7 Example of abnormal frequency with an external Rfext

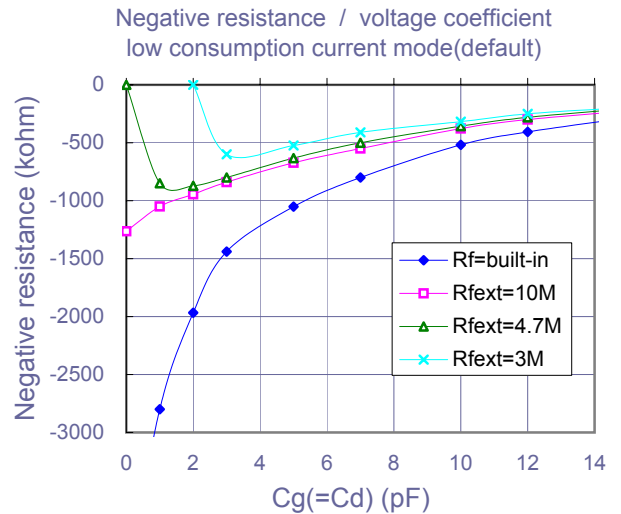


Figure 8 Example of abnormal oscillation behavior with an external Rfext

2. XCIN oscillation circuit and recommended load capacitance

XCIN oscillation circuit consists of an excellent power saving circuit which realizes stable oscillation at low amplitude.

The R8C/Lx series are a range of super low power consumption microcontrollers, fitting the needs of power reduction at stand-by mode for longer battery life. Resonators with small load capacitance (such as the VT-200-FL series), manufactured using SII innovative techniques, maximize XCIN oscillation circuit's performance. In addition, the VT-200-FL_4.4pF will be offered, realizing a 50% power consumption reduction in oscillation and a 2 x super high speed oscillation start-up time.

For your design reliability, please refer to Table 1 which shows the performance of the XCIN oscillation circuit and the recommended load capacitance for each resonator.

Resonators for small load capacitance are best fitted for super low power oscillation. Utmost performance to fulfill your expectations has been realized.

Table 1 Performance of XCIN oscillation circuit and load capacitance for a resonator

*R1max=50kΩ

Low_CL series	Vcc	Rd	Cg	Cd	Cd charge current (super low power)	Start up time (High speed)	Oscillation allowance*
6.0pF	5.0V	0Ω	5pF typ	5pF typ	210nA typ	0.68sec typ	17times typ
	3.3V	0Ω	5pF typ	5pF typ	180nA typ	0.76sec typ	14times typ
4.4pF	5.0V	330kΩ	2pF typ	3pF typ	115nA typ	0.37sec typ	22times typ
	3.3V	330kΩ	2pF typ	3pF typ	100nA typ	0.43sec typ	19times typ

3. Value tolerance of external capacitors (±5%) and frequency stability

XCIN oscillation circuit has the superior feature that frequency fluctuation is small (-0.21ppm to +0.12ppm) to the power supply voltage range (1.8V to 5.5V). Frequency stability depends largely on capacitance tolerance of external capacitors.

Frequency stability becomes a significant issue, especially in a "super low power consumption" oscillation circuit.

We offer the possibility of frequency as stable as that of large load capacitance (12.5pF) or even better by appropriate combinations between stray capacitance, Cs, and a resonator for small load capacitance to reduce the frequency deviation which will be expanded by external capacitors with capacitance value tolerance (±5%).

In a low frequency oscillation circuit as shown Figure 9, its load capacitance, CL, value can be expressed by the sum of

$$CL = Cs + C_{ext} = Cs + \frac{C_g \times C_d}{C_g + C_d} \quad (\text{pF})$$

external capacitors with capacitance tolerance (±5%), Cext, and stray capacitance, Cs. Stray capacitance, Cs, can be evaluated with high accuracy by measuring the frequency at the 32kHz clock monitoring terminal.

Capacitance, Cs, existing over a mounting circuit board, is a unique value which is determined by materials of the circuit board (dielectric constant), signal patterns (n layer-structure), and the IC's internal capacitance. It is difficult to specify (predict) the Cs, but accumulated data in the past makes it possible to estimate that value.

The accumulated data shows us the range of stray capacitance lies intensively in $2\text{pF} \leq Cs (=CL - C_{ext}) \leq 4\text{pF}$. These empirical values are assumed to be effective.

Under $2\text{pF} \leq Cs \leq 4\text{pF}$, the relationship between oscillation frequency, fosc, and nominal frequency, fo, is shown below:

$$\Delta f = f_{osc} - F_0 = f_r \times \left[\frac{C_1}{2(C_0 + C_s + C_{ext})} - \frac{C_1}{2(C_0 + C_L)} \right]$$

When $CL = Cs + C_{ext}$, $f_{osc} = F_0$.

If capacitance tolerance of Cext (±ΔCext) exists,

$$CL > Cs + C_{ext} - \Delta C_{ext}, \Delta f = f_{osc} - F_0 > 0 \text{ (Advance)}$$

$$CL < Cs + C_{ext} + \Delta C_{ext}, \Delta f = f_{osc} - F_0 < 0 \text{ (Delay)}$$

the above formulas show that frequency deviation becomes apparent and frequency stability deteriorates (increase of frequency off-set).

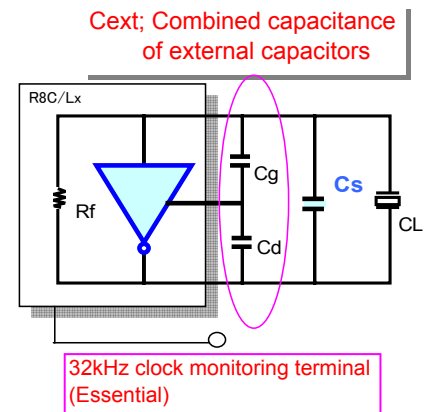


Figure 9 Value of load capacitance, CL, in a low frequency oscillation circuit

C1 : Motional capacitance
C0 : Shunt capacitance

Figure10 shows the association chart of maximum deviation, $(\Delta f)_{CL}$, with capacitance tolerance of C_{ext} ($\pm 5\%$).

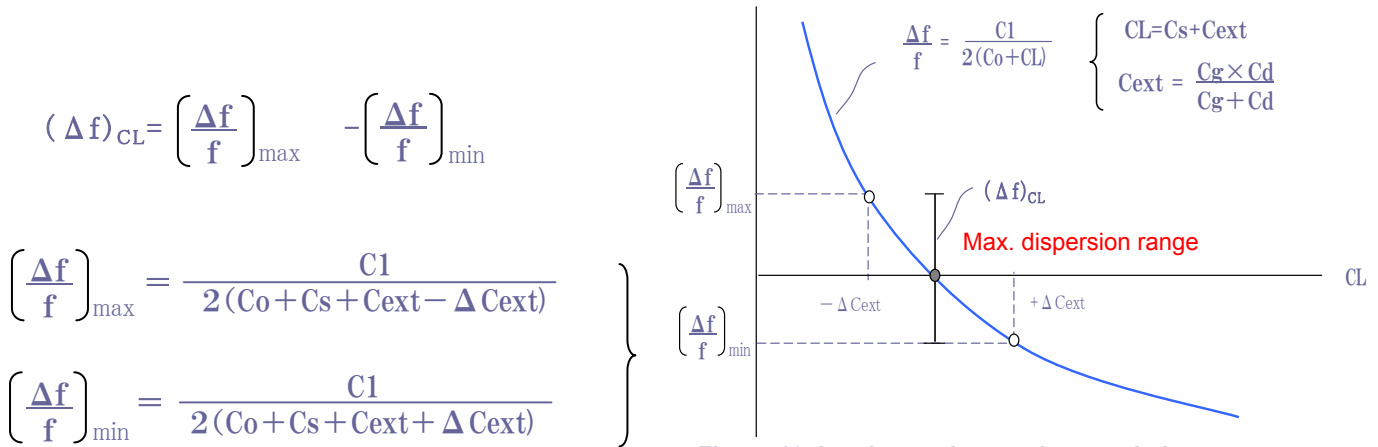


Figure 10 Load capacitance characteristics of frequency

Figure 11 shows maximum deviations of frequency, $(\Delta f)_{CL}$, with capacitance value tolerance ($\pm 5\%$) when each assumed stray capacitance value as parameters.

Maximum deviation with a resonator for small load capacitance (e.g., 9pF) has an increasing tendency when compared with a resonator for large load capacitance (e.g., 12.5pF). Maximum deviation with a resonator for further smaller load capacitance, 6pF or less, has a decreasing tendency, and there is a frequency stability zone where frequency can be stabilized as good as or even better than that for 12pF.

In addition to unprecedented low power consumption, it has been proven that small load capacitance (Low_CL) can realize frequency stability which is equal or superior to the one with a resonator for large load capacitance by utilizing stray capacitance, C_s , proactively.

Maximum deviations of frequency, $(\Delta f)_{CL}$, with capacitance tolerance of C_{ext} ($\pm 5\%$)

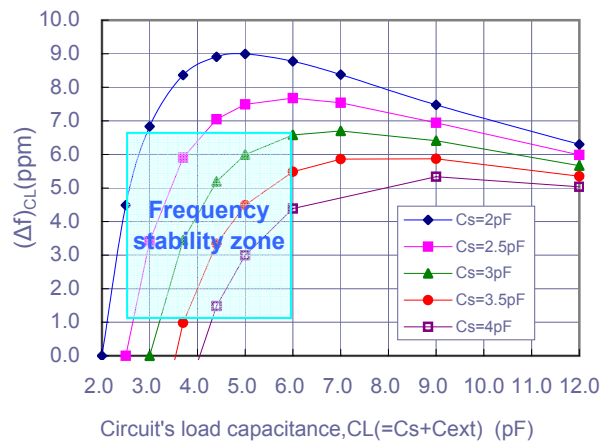


Figure 11 Maximum frequency deviations with capacitance tolerance

4. Combination with stray capacitance which minimizes maximum tolerance (examples for actual use)

$(\Delta f)_{CL}$ is expanded by capacitance tolerance of external capacitors, C_{ext} ($\pm 5\%$). Optimal combination between stray capacitance, C_s , and a resonator for small load capacitance can realize $(\Delta f)_{CL}$ which makes frequency more stable than $(\Delta f)_{12.5pF}$ (at $CL=12.5pF$). Combination examples for actual use between stray capacitance ($2pF \leq C_s \leq 4pF$) and low $CL (< 6pF)$, which satisfy $(\Delta f)_{12.5pF} \geq (\Delta f)_{CL}$, is shown in Table 2. Capacitance step, 0.1pF ($\leq 9.9pF$) of the temperature compensation type GRM series equivalent is recommended for C_{ext} in actual use.

Table 2 (Examples for actual use) Low CL specifications <6pF, minimizing maximum deviation

Cs+Cext Combi.	Stray Cap. Cs(pF)	Low_CL (pF)	Cext(pF)		Max. dev. $(\Delta f)_{CL}$ (ppm)	Std. CL (pF)	Cext(pF)		Max. dev. $(\Delta f)_{CL}$ (ppm)
			min.	max.			min.	max.	
set.1	2.0	3.0	0.95	1.05	6.8	12.5	9.98	11.03	6.1
set.2	2.5	3.7	1.14	1.26	5.9	12.5	9.50	10.50	5.8
set.3	3.0	3.7	0.67	0.74	3.4	12.5	9.03	9.98	5.6
set.4	3.5	4.4	0.86	0.95	3.3	12.5	8.55	9.45	5.3
set.5	4.0	4.4	0.38	0.42	1.5	12.5	8.08	8.93	5.0

Note) When $C_g=C_d=C$, $C_{ext}=C/2$ (for example, if $C_{ext}=0.9pF$, 2 capacitors with $C=1.8pF$ are mounted)