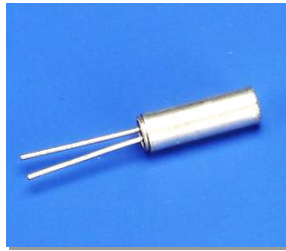


# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0495GK-GAK-AX] QFP(12x12) 0.50mm pitch

Measurement conditions : 1.8V(reference), 3.0V to 5.0V

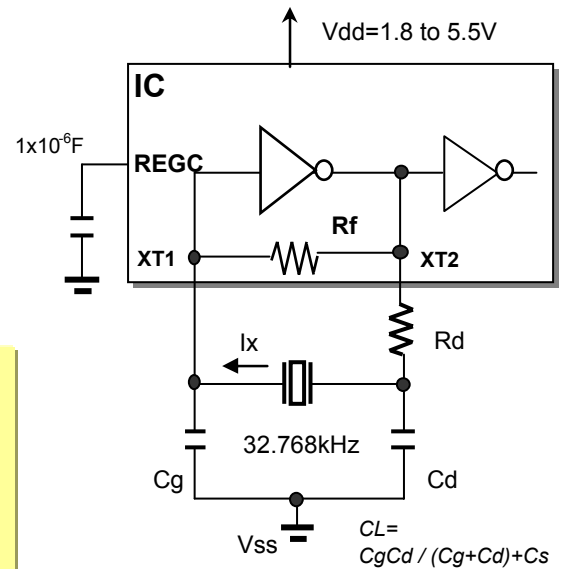
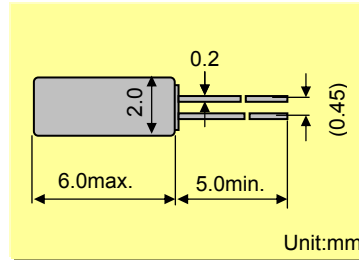


Model	:VT-200
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10 <sup>6</sup>
Load capacitance	:CL=12.5pF
Equivalent series resistance	:R1=50kohm max
Max. drive level	:DL=1x10 <sup>6</sup> W max
Level of drivel	:DL=0.1x10 <sup>6</sup> W typ

## FEATURES

- 1.Compact tubular package
- 2.Photolithographic process
- 3.Excellent shock resistance and environmental characteristics.
- 4.Real time clocks, Timers, Portable applications

## DIMENSIONS(VT-200)



Remark)  $I_x$  : current through crystal

MODEL:VT-200 12.5pF with uPD78F0495GK at 25°C

Key specifications	Vdd=1.8V	3.0 to 5.0V	Remarks
Current control resistance : $R_d$ ( k ohm )	0	0	Control drive level & secure phase margin
Capacitance at gate : $C_g$ ( pF )	22	22	Optimal capacity in response to CL
Capacitance at drain : $C_d$ ( pF )	18	18	( $CL = C_d // C_g + \text{stray capacitance}$ )

Circuit characteristics ( at 25°C )	Vdd=1.8V	3.0 to 5.0V	Remarks
Matching Accuracy : $df / f$ ( $\times 10^{-6}$ )	-3.4	-0.6	Frequency offset volume at specified Vdd
Voltage Fluctuation : $+/-df / V$ ( $\times 10^{-6}$ )	1.0	0.0	Vdd +/-10% ( Standard operating voltage range )
Drive Level : DL ( $\times 10^{-6}$ W )	0.13	0.27	$DL = I_x^2 R_e < 1 \times 10^{-6}$ W, $R_e = R_1( 1 + C_o / CL )^2$
Negative resistance : $ -RL $ ( kohm )	144	234	5 times larger than $R_{1MAX}$
Oscillation allowance : M ( times )	2.9	4.7	Judgemental standard of oscillation stability
Voltage of oscillation start : $V_{start}$ ( V )	1.59	1.59	
Voltage of oscillation stop : $V_{stop}$ ( V )	1.58	1.58	
Oscillation start up time : $T_s$ ( sec )	3.21	1.39	Time to reach 90% of output level

Temperature characteristics of circuit		Vdd=1.8V	3.0 to 5.0V	Remarks
at -40°C	Variation : $df / T$ ( $\times 10^{-6}$ )	-143	-143	Typ.Tp=25°C ( $K = -3.5 \times 10^{-8} / ^\circ C^2$ )
at +85°C	Variation : $df / T$ ( $\times 10^{-6}$ )	-127	-127	Typ.Tp=25°C ( $K = -3.5 \times 10^{-8} / ^\circ C^2$ )

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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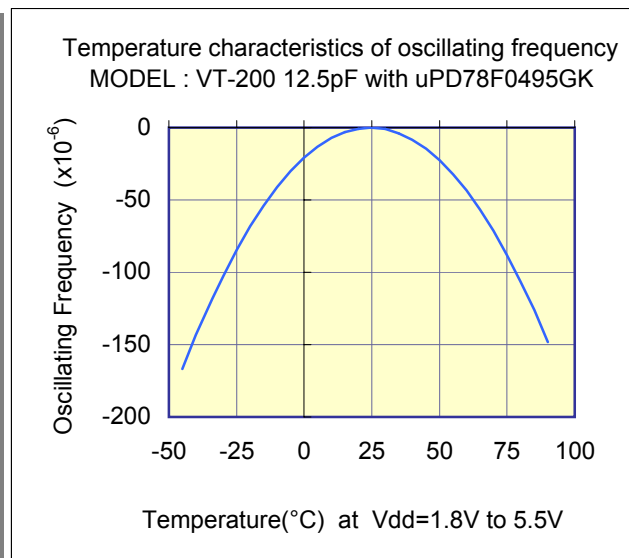
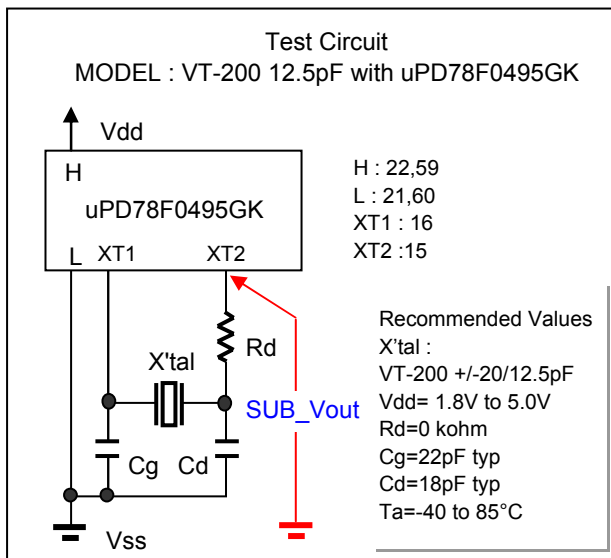
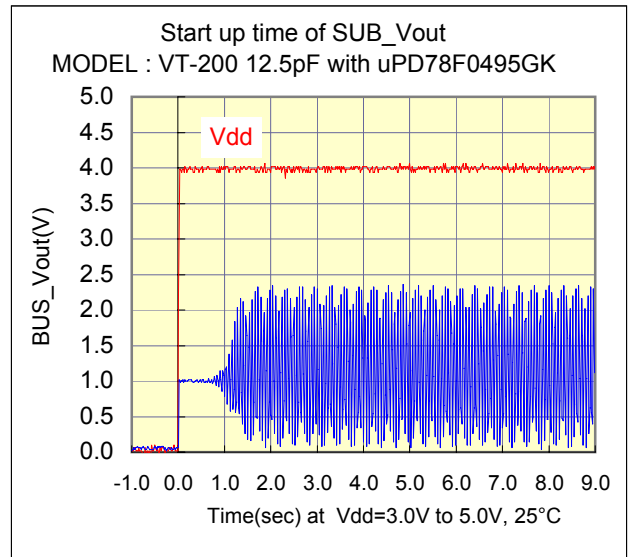
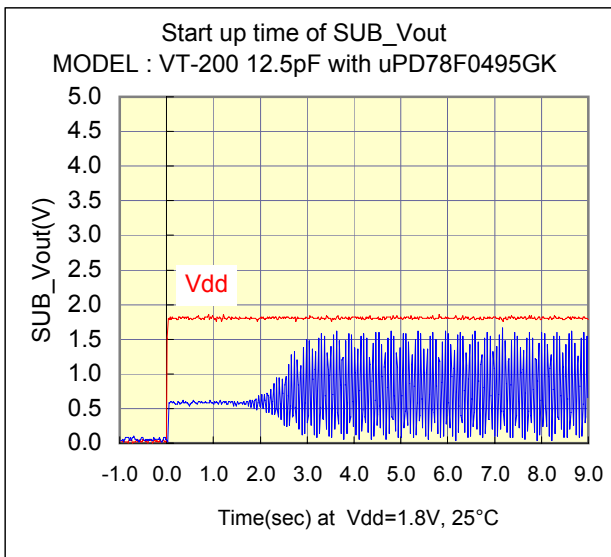
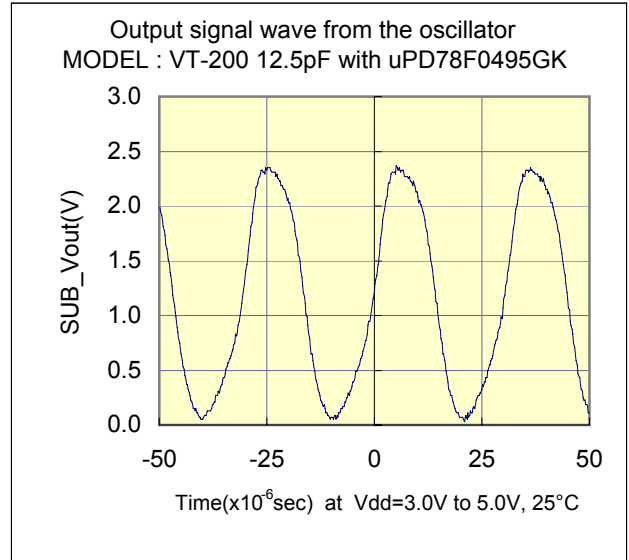
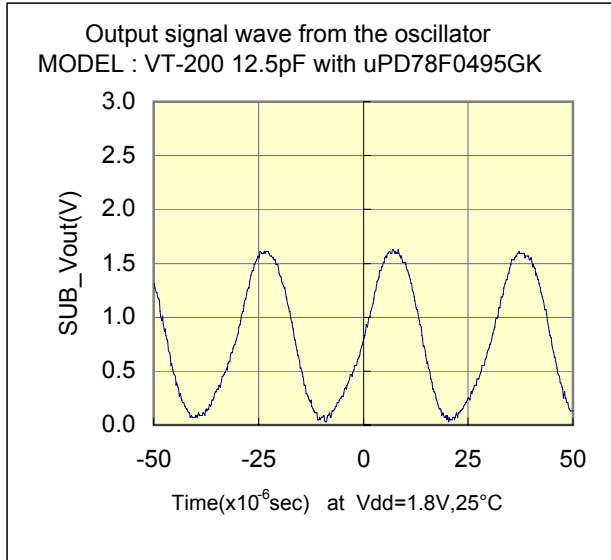
# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0495GK-GAK-AX] QFP(12x12) 0.5mm pitch

Measurement conditions : 1.8V(reference), 3.0V to 5.0V



## Test Data



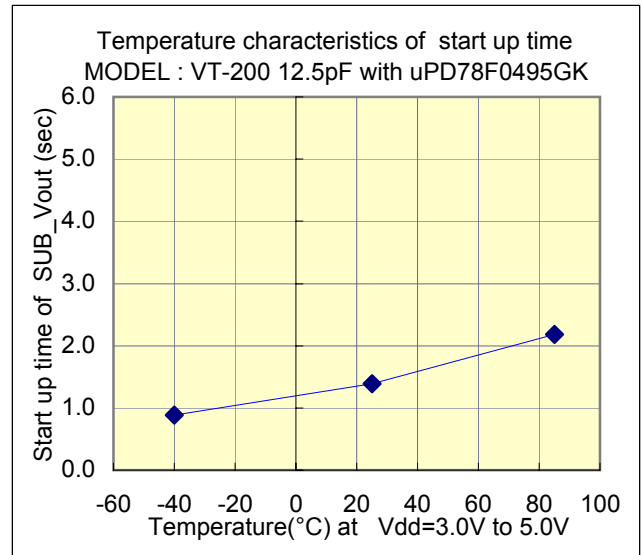
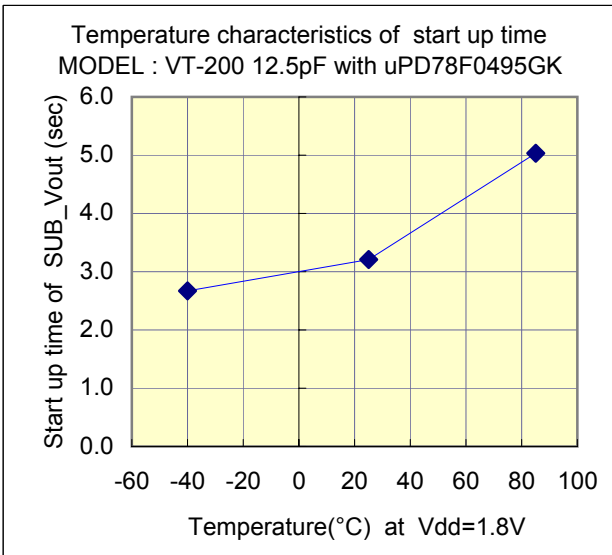
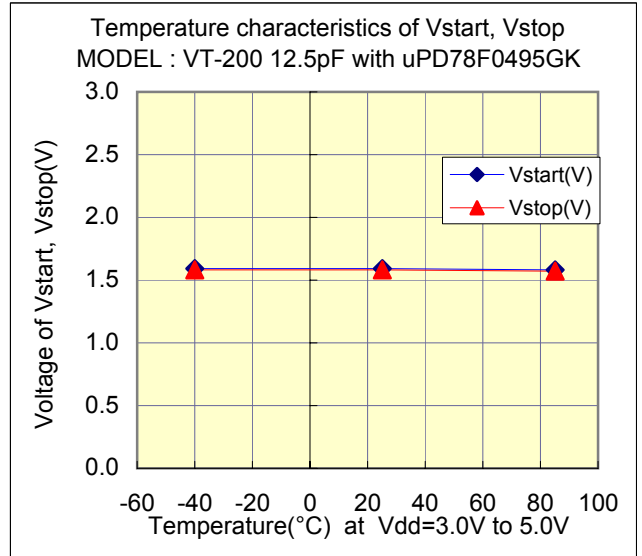
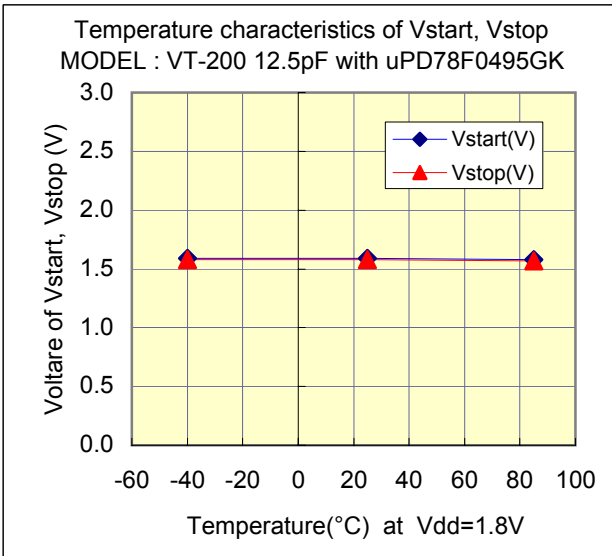
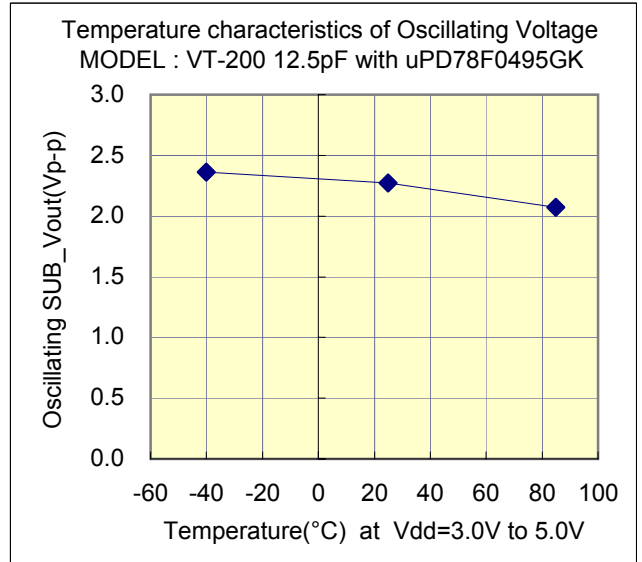
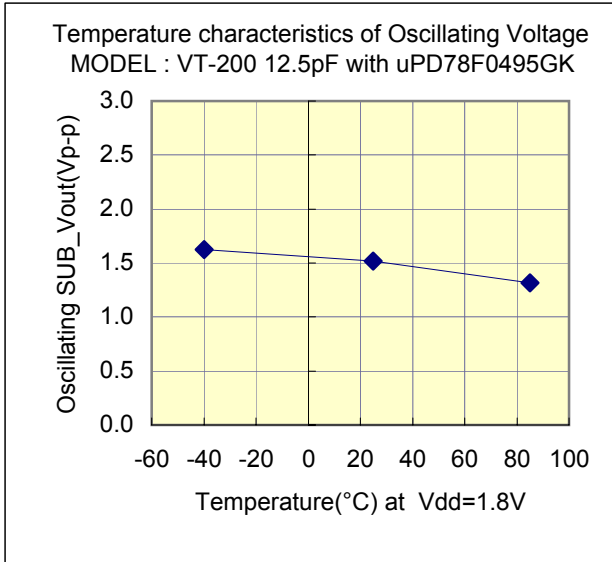
# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0495GK-GAK-AX] QFP(12x12) 0.50mm pitch

Measurement conditions : 1.8V(reference), 3.0V to 5.0V



## Test Data : Temperature characteristics



# Evaluation of Subsystem Clock Oscillation Circuit

[ $\mu$ PD78F0495GK-GAK-AX] QFP(12x12) 0.50mm pitch

Measurement conditions : 1.8V(reference), 3.0V to 5.0V



## Referential components layout(see Figure 1)

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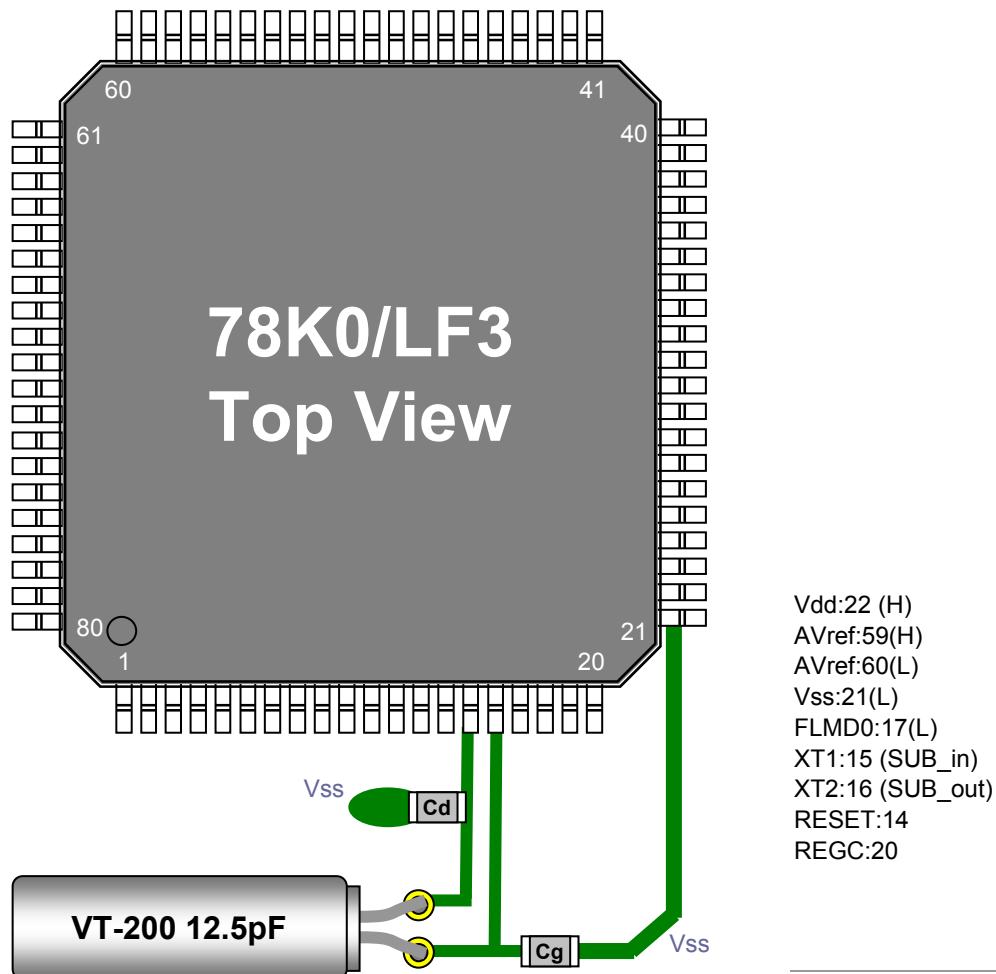


Figure 1 Referential components layout

## Notes for Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB\_in and SUB\_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

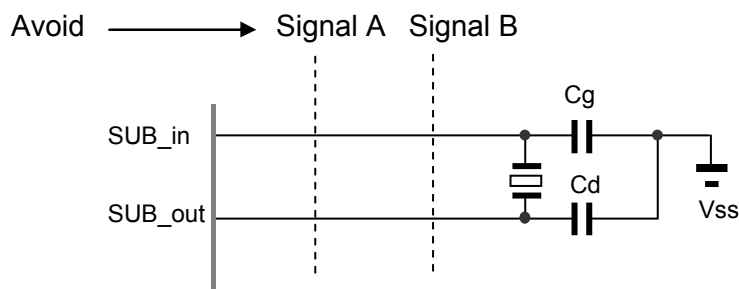


Figure 2 Example of Incorrect Board Design

**Remark** When using the subsystem clock, insert resistors  $R_d$  in series on the SUB\_out side.

# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0495GK-GAK-AX] QFP(12x12) 0.50mm pitch

Measurement conditions : 1.8V(reference), 3.0V to 5.0V



## [Evaluation Sample : VT-200 12.5pF at 25°C]

SAMPLE	No.	CL( pF )	Fo( Hz )	fr( Hz )	R1( kohm )	Co( pF )	C1( fF )	Q( k )
VT-200 12.5pF	1	12.5	32768.11	32765.28	27.4	0.91	2.319	76.5
	2	12.5	32768.09	32765.24	26.9	0.89	2.333	77.4
	3	12.5	32768.34	32765.45	29.9	0.93	2.368	68.6

## [IC Test Data : IC Sample Rd=0 kohm,Cg=22pF,Cd=18pF at 25°C]

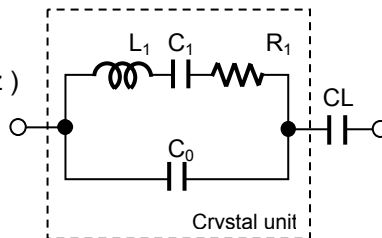
Vdd(V)	IC Samples	Fosc( Hz )	df / f( x10 <sup>-6</sup> )	DL(x10 <sup>-6</sup> W)	-RL  ( kohm )	Vstart( V )	Ts(sec)
3 to 5	CC	32768.32	-0.62	0.27	234.49	1.59	1.39
	LL	32768.30	-1.29	0.26	254.49	1.59	1.24
	LH	32768.28	-1.68	0.27	214.49	1.60	1.56
	HL	32768.30	-1.29	0.26	254.49	1.60	1.21
	HH	32768.33	-0.28	0.27	234.49	1.59	1.44

## [IC Test Data : IC Sample Rd=0 kohm,Cg=22pF,Cd=18pF at 25°C]

Vdd(V)	IC Samples	Fosc( Hz )	df / f( x10 <sup>-6</sup> )	DL(x10 <sup>-6</sup> W)	-RL  ( kohm )	Vstart( V )	Ts(sec)
1.8	CC	32768.23	-3.39	0.13	144.49	1.59	3.21
	LL	32768.24	-3.15	0.14	154.49	1.59	2.44
	LH	32768.20	-4.25	0.09	125.49	1.60	4.30
	HL	32768.24	-3.15	0.14	154.49	1.60	2.45
	HH	32768.25	-2.72	0.11	134.49	1.59	3.60

### Remark ( see figure 3 )

$$Fo = fr \times \{ C1 / ( 2 \times ( Co + CL ) ) + 1 \} \text{ ( Hz )}$$



Fo : Load resonance frequency  
fr : Resonance frequency  
R1 : Motional resistance  
C1 : Motional capacitance  
Co : Shunt capacitance  
CL : Load Capacitance

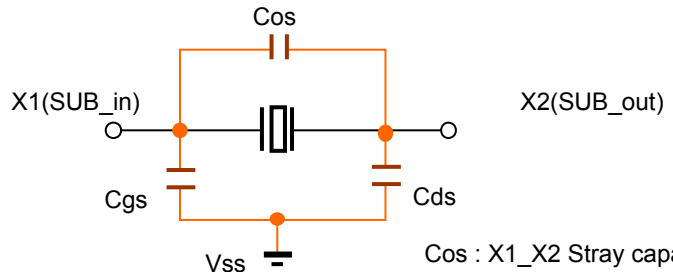
Figure 3 Equivalent circuit of crystal unit, and CL

### Remark ( see figure 4 )

Approximate formula of the load capacitance of the circuit CL.

$$CL = Cg \times Cd / ( Cg + Cd ) + Cs \text{ ( pF )}$$

Where Cs(=2 to 4pF) Stands for stray capacitance of the circuit.



Cos : X1\_X2 Stray capacitance  
Cgs : X1\_Vss Stray capacitance  
Cds : X2\_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.

# Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0495GK-GAK-AX] QFP(12x12) 0.50mm pitch

Measurement conditions : Vdd=1.6V to 5.5V at 25°C

## Referential Data : Voltage characteristics

