

Evaluation of Subsystem Clock Oscillation Circuit

[uPD78F0495GK-GAK-AX] QFP(12x12) 0.50mm pitch

Measurement conditions : 1.8V(reference), 3.0V to 5.0V

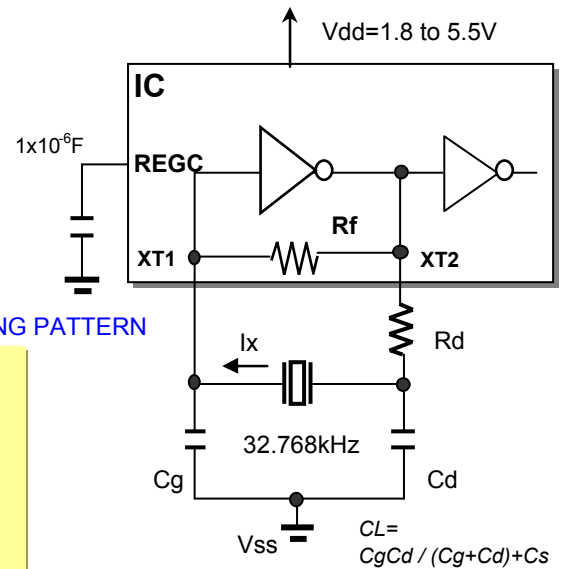
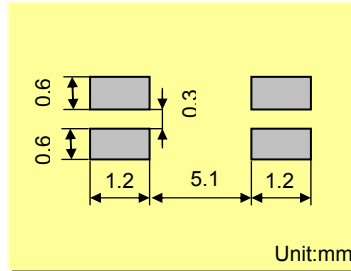


Model	:SSP-T7
Frequency	:Fo=32.768kHz
Frequency tolerance	:dF/Fo= +/-20x10 ⁶
Load capacitance	:CL=12.5pF
Equivalent series resistance	:R1=65kohm max
Max. drive level	:DL=1x10 ⁶ W max
Level of drive	:DL=0.1x10 ⁶ W typ

FEATURES

- 1.Ultra thin type with 1.4mm Max.
- 2.SMD type suitable for automatic & high density surface mounting.
- 3.Plastic mold package containing highly reliable tubular type quartz crystal.
- 4.Excellent shock and heat resistance.
- 5.Cellular phones,PDA,Radio communication equipment, Portable applications etc.

RECOMMENDED SOLDERING PATTERN



Remark) I_x : current through crystal

MODEL:SSP-T7 12.5pF with uPD78F0495GK at 25°C

Key specifications	Vdd=1.8V	3.0 to 5.0V	Remarks
Current control resistance : R_d (k ohm)	0	0	Control drive level & secure phase margin
Capacitance at gate : C_g (pF)	22	22	Optimal capacity in response to CL
Capacitance at drain : C_d (pF)	18	18	($CL = C_d // C_g + \text{stray capacitance}$)

Circuit characteristics (at 25°C)	Vdd=1.8V	3.0 to 5.0V	Remarks
Matching Accuracy : df / f ($\times 10^{-6}$)	-2.7	-0.6	Frequency offset volume at specified Vdd
Voltage Fluctuation : $+/-df / V$ ($\times 10^{-6}$)	0.8	0.0	Vdd +/-10% (Standard operating voltage range)
Drive Level : DL ($\times 10^{-6}$ W)	0.15	0.34	$DL = I_x^2 R_e < 1 \times 10^{-6}$ W, $R_e = R_1 (1 + C_o / CL)^2$
Negative resistance : $ -RL $ (kohm)	144	244	5 times larger than R_{1MAX}
Oscillation allowance : M (times)	2.2	3.7	Judgemental standard of oscillation stability
Voltage of oscillation start : V_{start} (V)	1.60	1.60	
Voltage of oscillation stop : V_{stop} (V)	1.59	1.59	
Oscillation start up time : T_s (sec)	3.80	1.63	Time to reach 90% of output level

Temperature characteristics of circuit		Vdd=1.8V	3.0 to 5.0V	Remarks
at -40°C	Variation : df / T ($\times 10^{-6}$)	-137	-137	Typ.Tp=25°C ($K = -3.5 \times 10^{-8} / ^\circ C^2$)
at +85°C	Variation : df / T ($\times 10^{-6}$)	-133	-133	Typ.Tp=25°C ($K = -3.5 \times 10^{-8} / ^\circ C^2$)

The above mentioned value is only for your reference. The value is for the arbitrary samples and does not guarantee the product's characteristics. Please review and check above parameters at customer's end.

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We value the "takumi" spirit.

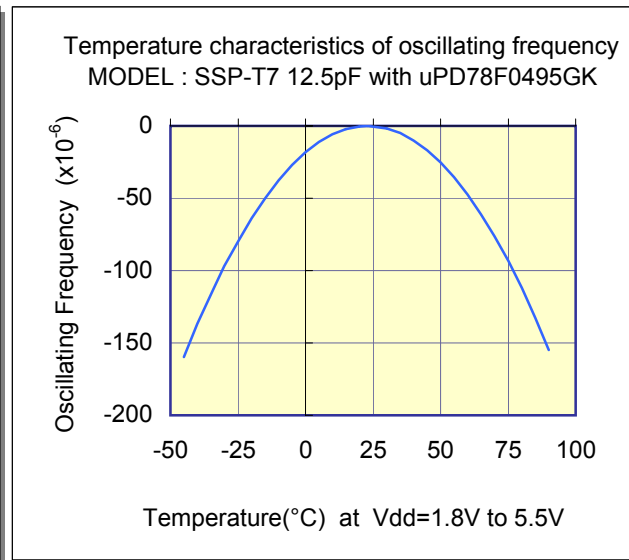
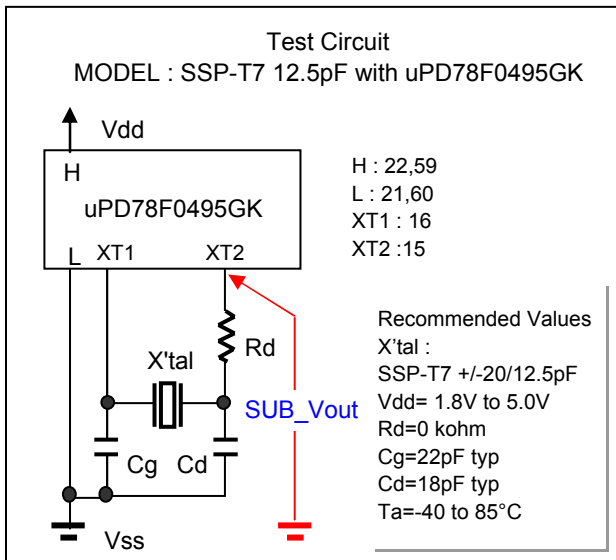
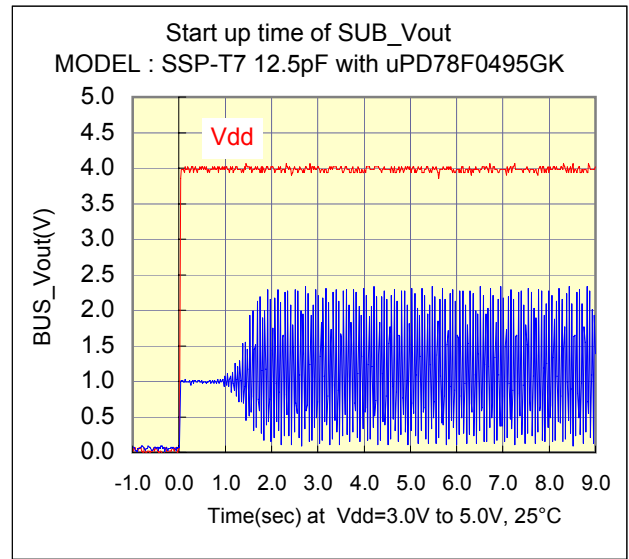
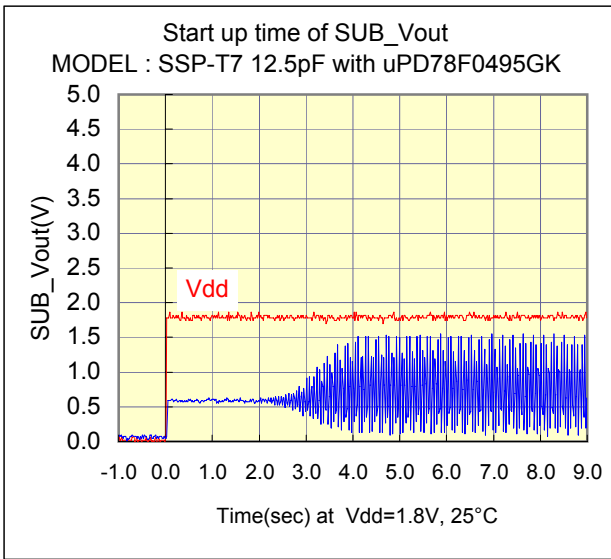
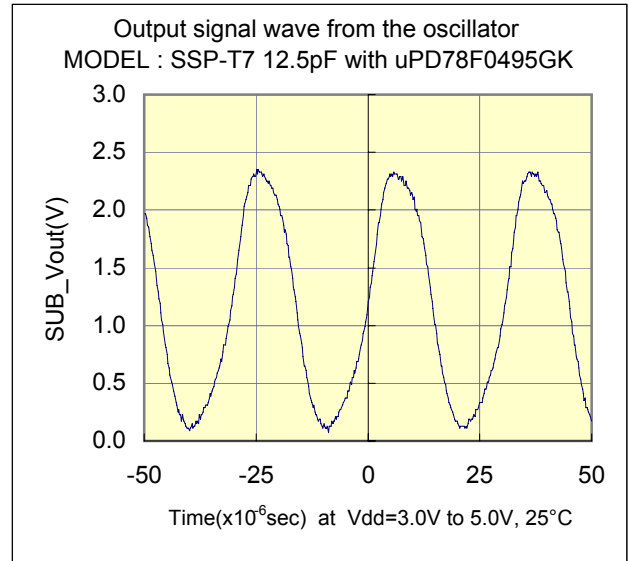
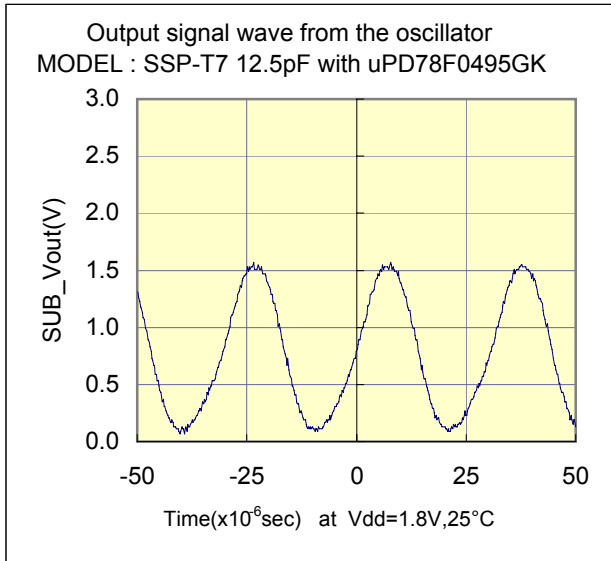
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Test Data



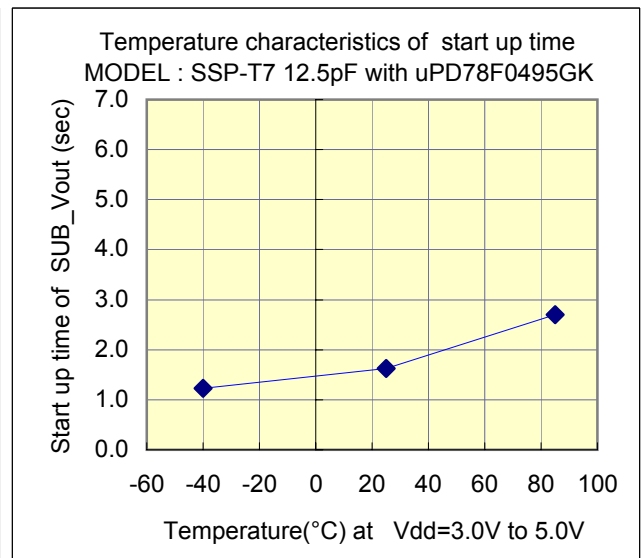
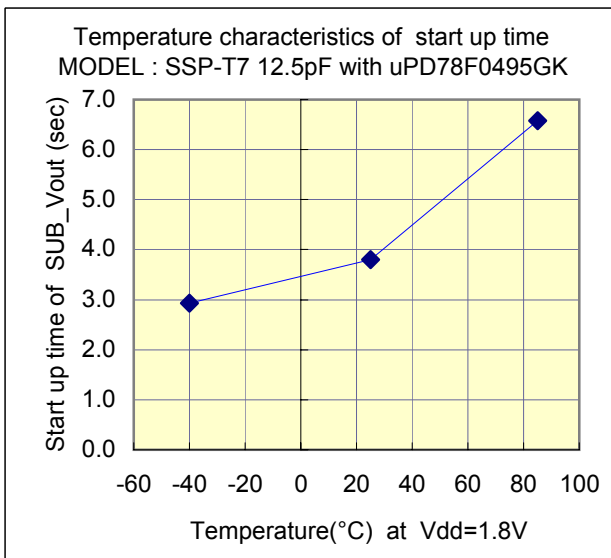
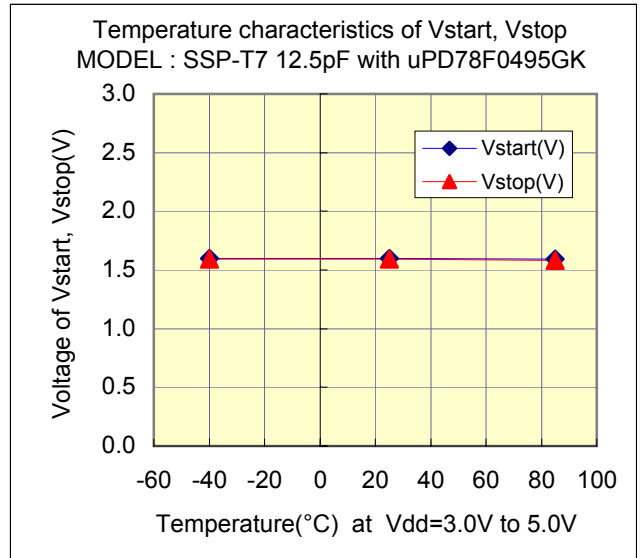
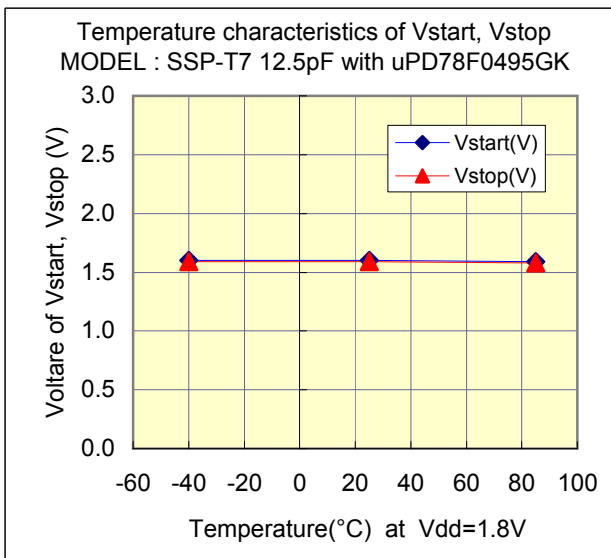
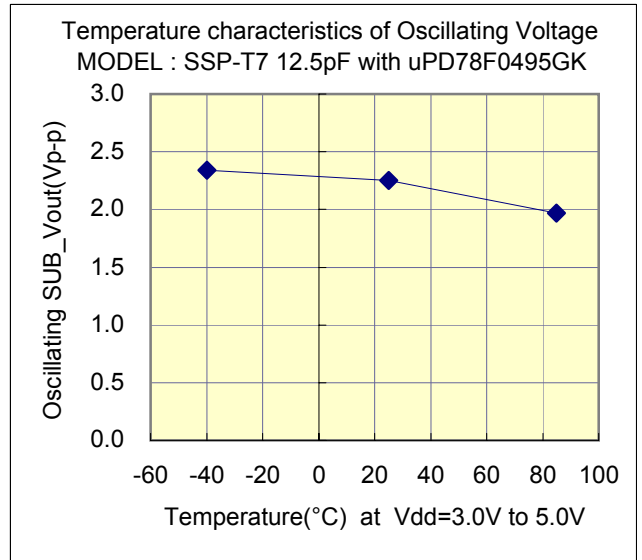
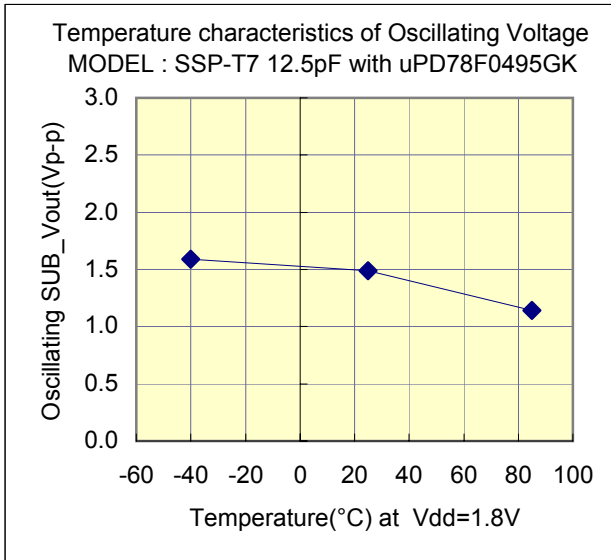
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Measurement conditions : 1.8V(reference), 3.0V to 5.0V



Test Data : Temperature characteristics



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Referential components layout(see Figure 1)

78K0/LF3 Supports Advanced Display Functions with Minimal Power Consumption

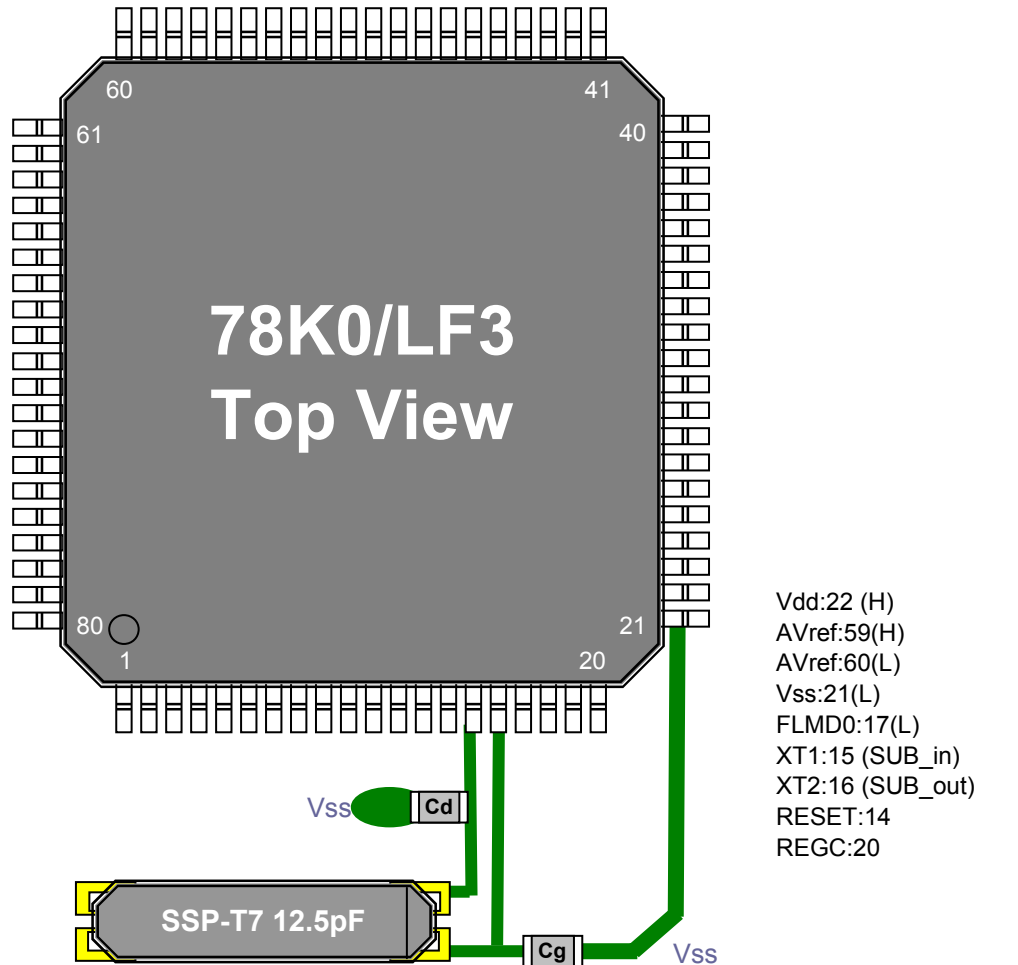


Figure 1 Referential components layout

Notes for Board Design

When using a crystal resonator, place the resonator and its load capacitors as close as possible to SUB_in and SUB_out pins.

Other signal lines should be routed away from the resonator circuit to prevent induction from interfering with correct oscillation (see figure 2).

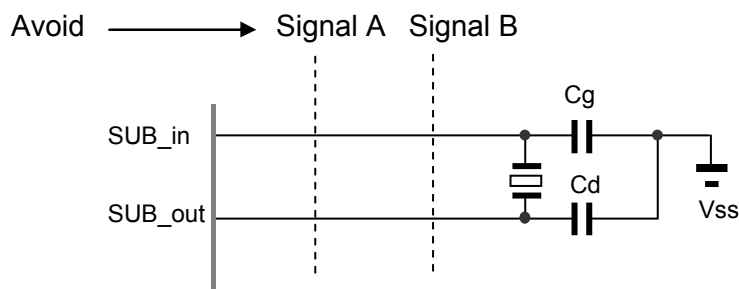


Figure 2 Example of Incorrect Board Design

Remark When using the subsystem clock, insert resistors R_d in series on the SUB_out side.

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Measurement conditions : 1.8V(reference), 3.0V to 5.0V



[Evaluation Sample : SSP-T7 12.5pF at 25°C]

SAMPLE	No.	CL(pF)	Fo(Hz)	fr(Hz)	R1(kohm)	Co(pF)	C1(fF)	Q(k)
SSP-T7 12.5pF	1	12.5	32768.10	32765.64	38.1	0.88	2.009	63.5
	2	12.5	32768.06	32765.60	45.1	0.84	2.003	53.8
	3	12.5	32768.16	32765.70	39.8	0.85	2.004	60.9

[IC Test Data : IC Sample Rd=0 kohm,Cg=22pF,Cd=18pF at 25°C]

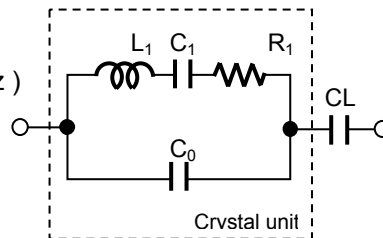
Vdd(V)	IC Samples	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart(V)	Ts(sec)
3 to 5	CC	32768.08	-0.61	0.34	243.63	1.60	1.63
	LL	32768.08	-0.52	0.32	263.63	1.59	1.36
	LH	32768.07	-0.92	0.33	223.63	1.60	1.78
	HL	32768.09	-0.34	0.31	263.63	1.60	1.40
	HH	32768.09	-0.21	0.33	243.63	1.59	1.70

[IC Test Data : IC Sample Rd=0 kohm,Cg=22pF,Cd=18pF at 25°C]

Vdd(V)	IC Samples	Fosc(Hz)	df / f(x10 ⁻⁶)	DL(x10 ⁻⁶ W)	-RL (kohm)	Vstart(V)	Ts(sec)
1.8	CC	32768.01	-2.75	0.15	143.63	1.60	3.80
	LL	32768.03	-2.29	0.17	163.63	1.59	2.86
	LH	32767.99	-3.30	0.11	134.63	1.60	4.92
	HL	32768.03	-2.29	0.17	163.63	1.60	2.69
	HH	32768.02	-2.59	0.13	143.63	1.59	4.22

Remark (see figure 3)

$$F_o = fr \times \{ C_1 / (2 \times (C_o + C_L)) + 1 \} \text{ (Hz)}$$



Fo : Load resonance frequency
fr : Resonance frequency
R1 : Motional resistance
C1 : Motional capacitance
Co : Shunt capacitance
CL : Load Capacitance

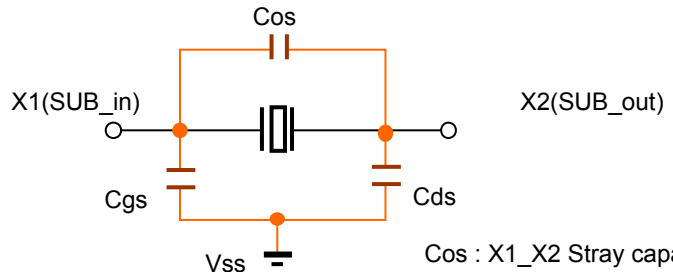
Figure 3 Equivalent circuit of crystal unit, and CL

Remark (see figure 4)

Approximate formula of the load capacitance of the circuit CL.

$$C_L = C_g \times C_d / (C_g + C_d) + C_s \text{ (pF)}$$

Where Cs(=2 to 4pF) Stands for stray capacitance of the circuit.



Cos : X1_X2 Stray capacitance
Cgs : X1_Vss Stray capacitance
Cds : X2_Vss Stray capacitance

Figure 4 Stray capacitance Cos,Cgs,Cds of the circuit

Resonator circuit constants will differ depending on the resonator element, stray capacitance in its interconnecting circuit, and other factors. Suitable constants should be determined in consultation with the resonator element manufacturer.



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Measurement conditions : Vdd=1.6V to 5.5V at 25°C

Referential Data : Voltage characteristics

